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# MS-7823

## Intel -SharkBay plamform Z87

mATX

Ver: 11(243.84x243.84)

CPU:

System Chipset:

Haswell LGA1150

Lynx Point Z87 co-lay H87 & B85

Onboard Chip:

HD Audio Codec:ALC892

LAN-RTL8111G

SIO:Nuvoton 6779D

Flash ROM: SPI 64 MB/128MB

Main Memory:

DDRIII (1066/1333/1600MHz) \* 4 (Dual Channel)

ACPI:

PWM:

UPI

ISL95812 3 Phase

Expansion Slots:

Other:

PCI Express (X16) Slot \* 1

SATA3.0 x6(PCH)

PCI Express (X1 ) Slot \* 2

REAL USB2.0 \*4

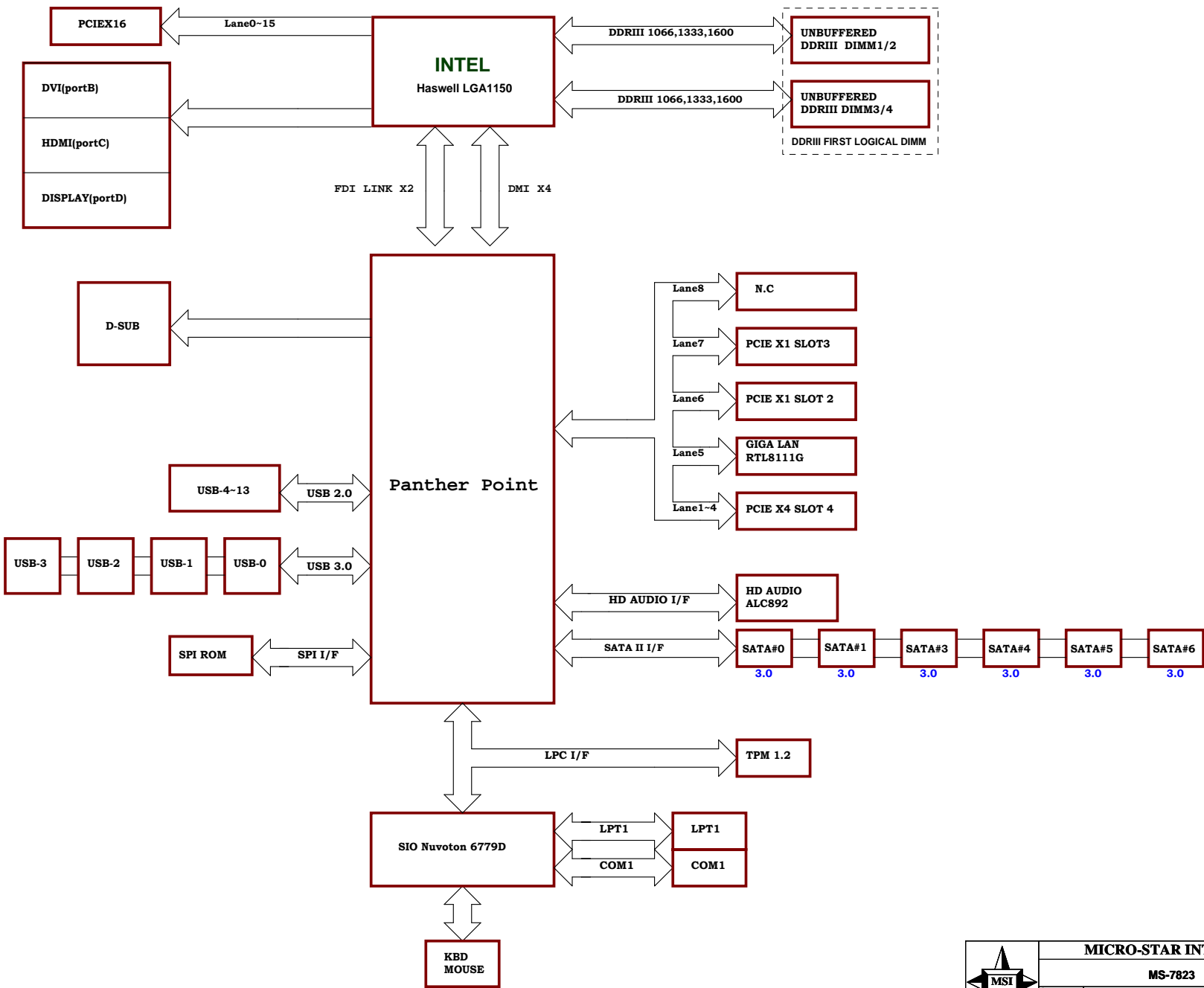
PCI Express (X4 ) Slot \* 1

FRONT USB2.0 \*6

REAL USB3.0 \*2

FRONT USB3.0 \*2

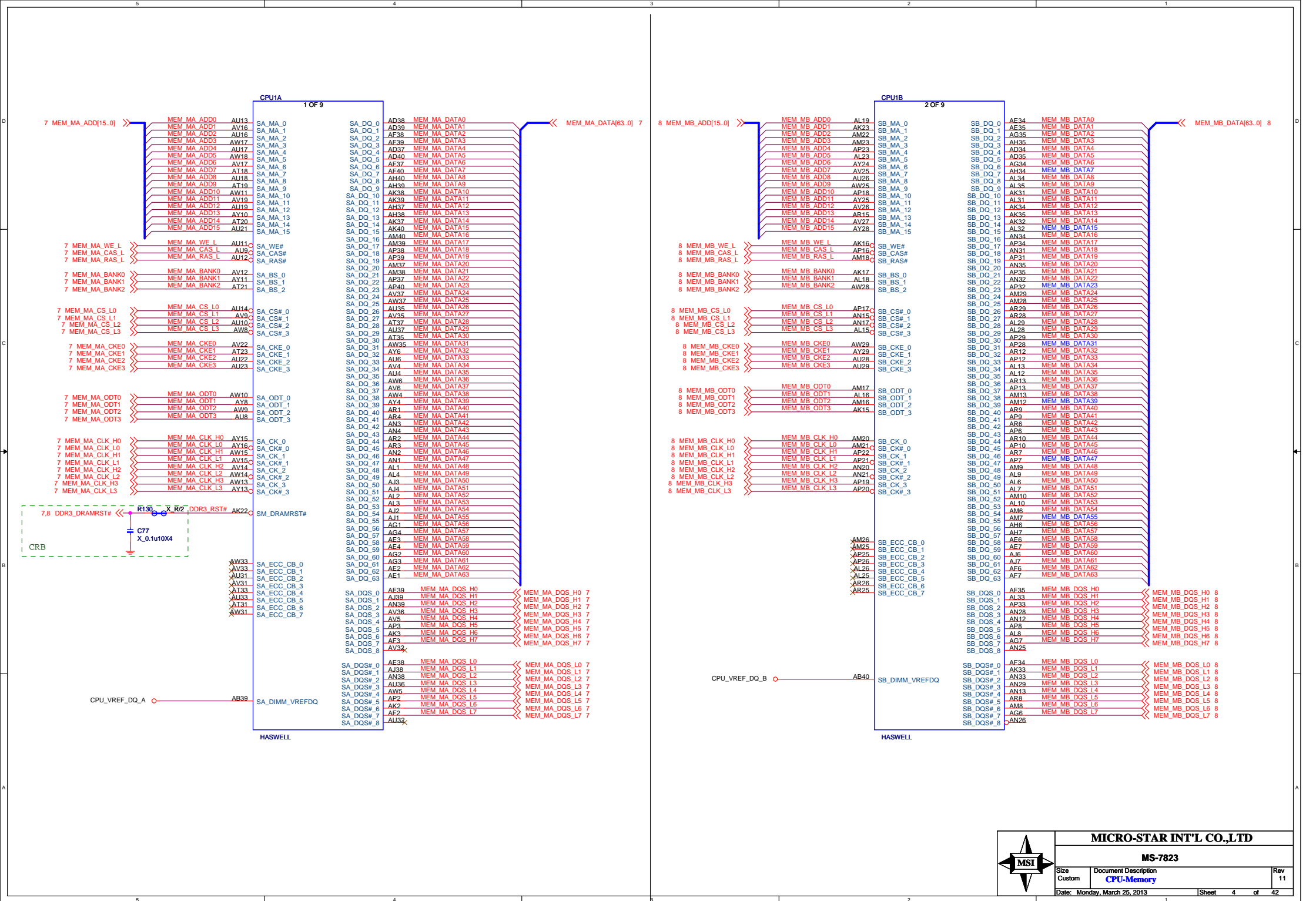
MS-7823 Block Diagram



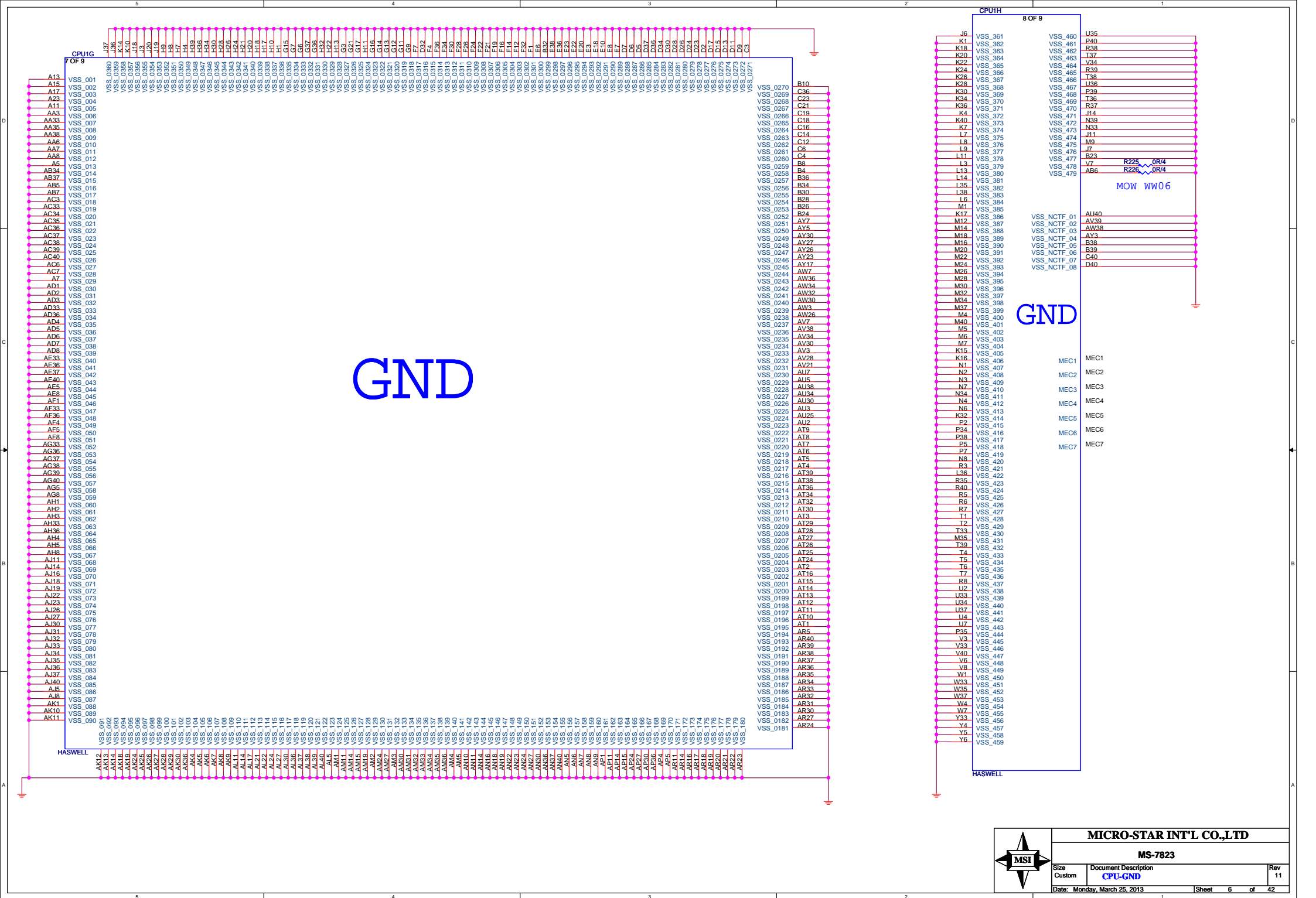
Slot Sequence:

- PCIE X16
- PCIE X1
- PCIE X1
- PCIE X16(X4)





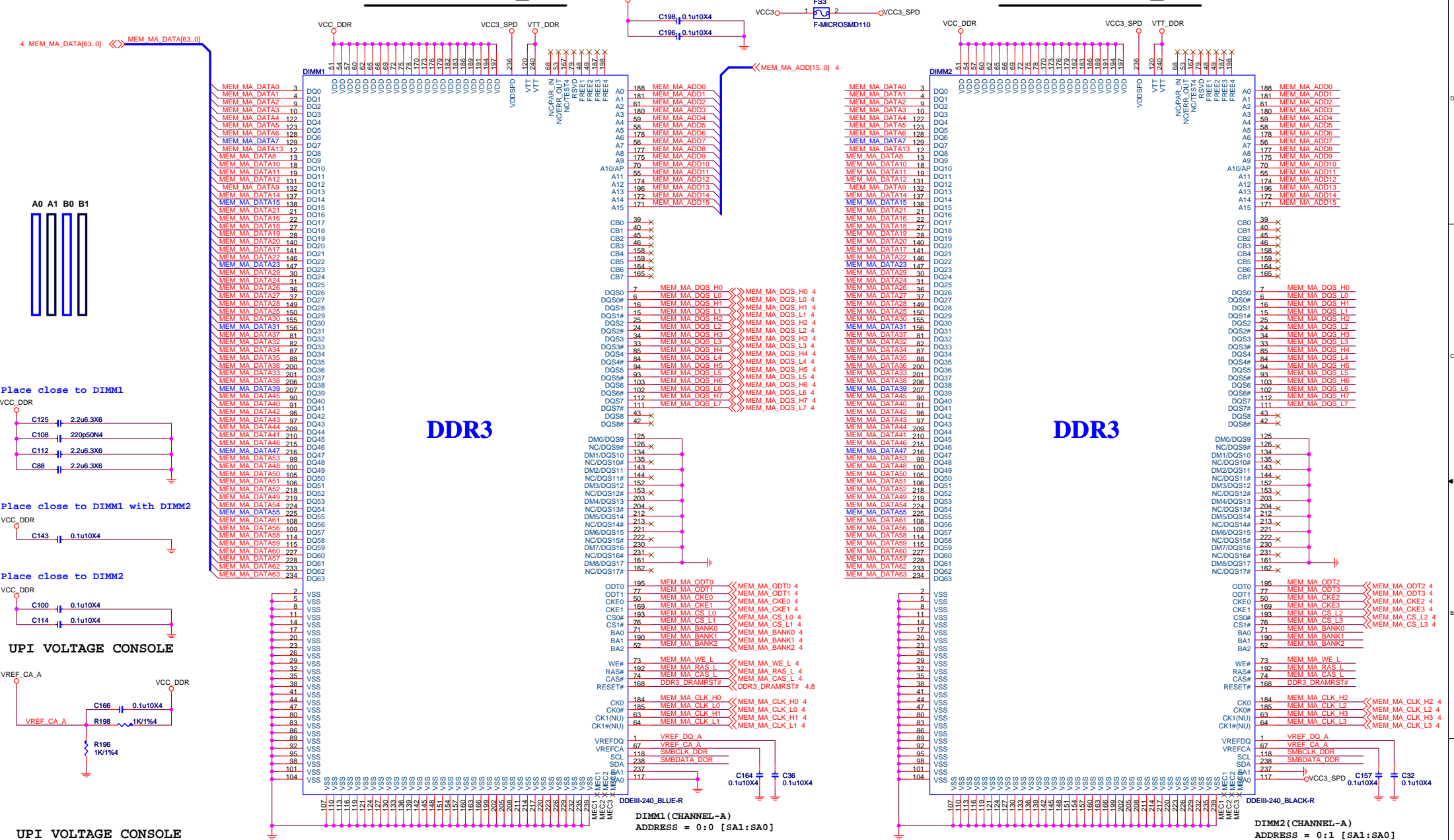






# DDRIII DIMM\_A0

# DDRIII DIMM\_A1



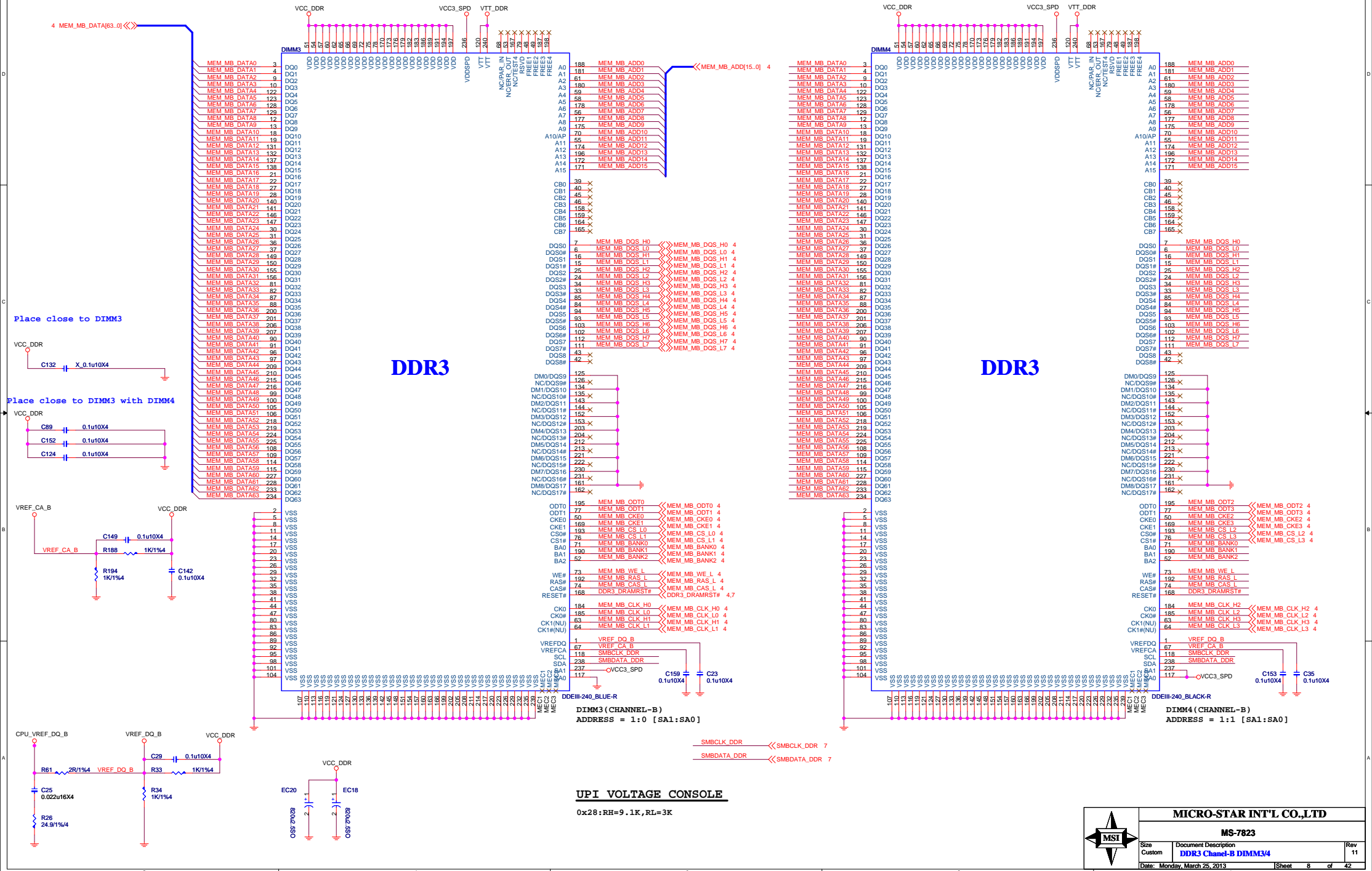
## UPI VOLTAGE CONSOLE

0x26: RH=18K, RL=13K

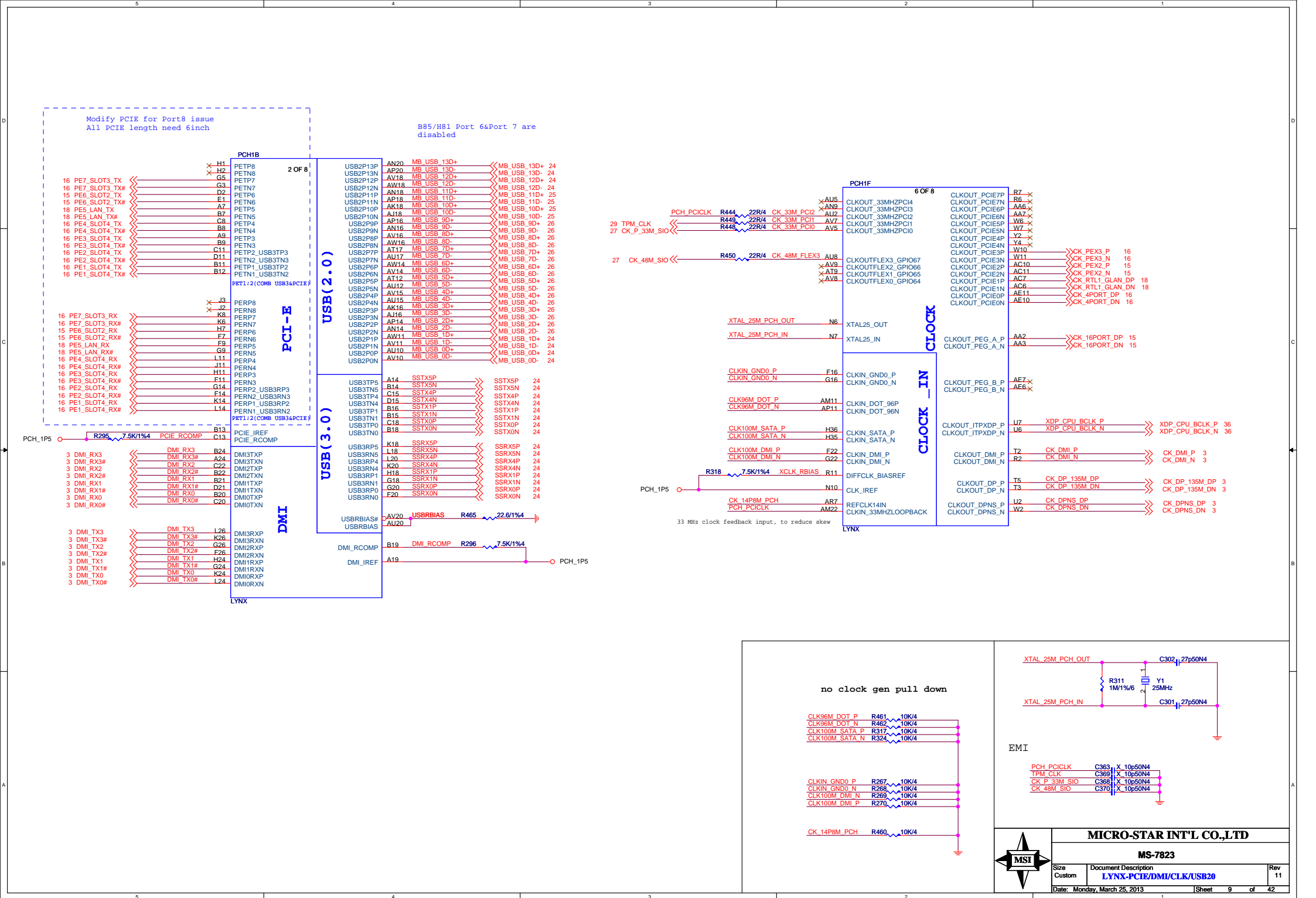
8 SMBCLK\_DDR >> SMBCLK\_DDR R250 33R/4 >> SMBCLK\_VCC 11,31,36  
8 SMBDATA\_DDR >> SMBDATA\_DDR R249 33R/4 >> SMBDATA\_VCC 11,31,36

# DDR3 DIMM\_B0

# DDR3 DIMM\_B1







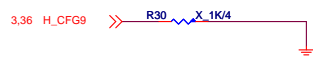
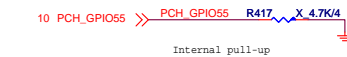
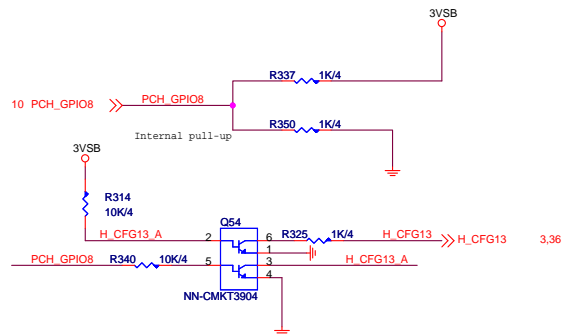
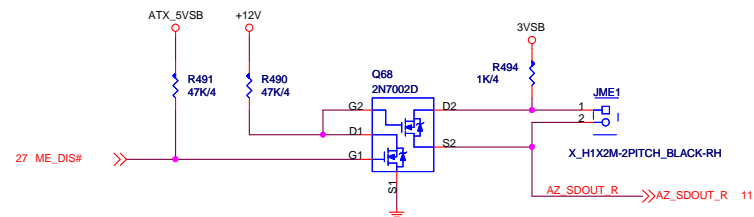
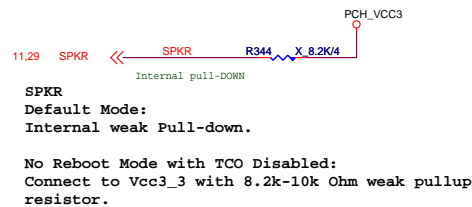




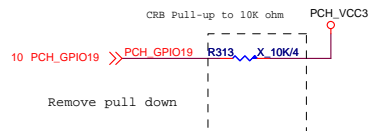
AF25 ;AD25 DT CRB0.7 ASW POWER

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For Sx power Cycling May Fail Due to SVID Logic Race Condition Within the Processor



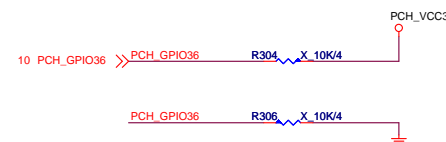
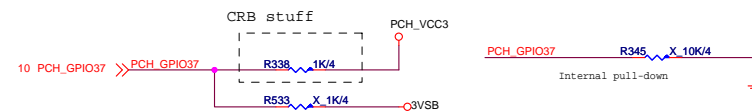
Default (SPI):  
Left both SATA1GP/GPIO19 and GPIO51 floating.  
No pull up required.

Boot from PCI:  
Connect SATA1GP/GPIO19 to ground with 1k Ohm pull-down resistor.  
Leave GPIO51 Floating.

Boot from LPC:  
Connect both SATA1GP/GPIO19 and GPIO51 to ground with 1k Ohm pull-down resistor.

BOOT DEVICE	GPIO51	GPIO19
LPC	0	0
SPI	1	1

Default

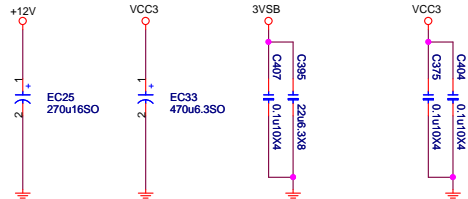
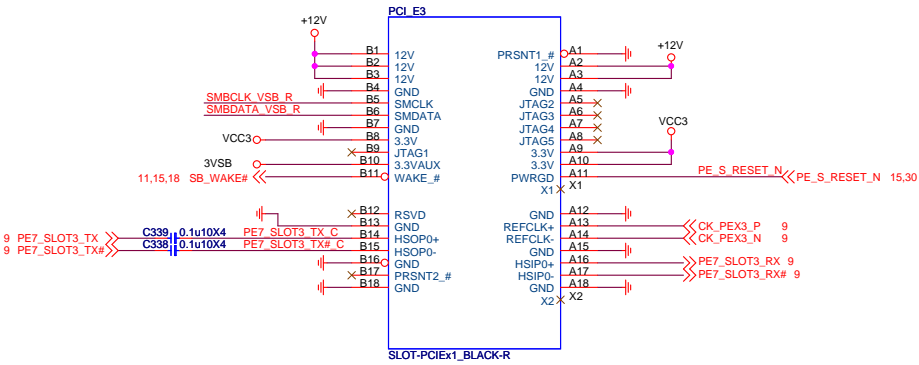


MICRO-STAR INT'L CO.,LTD		
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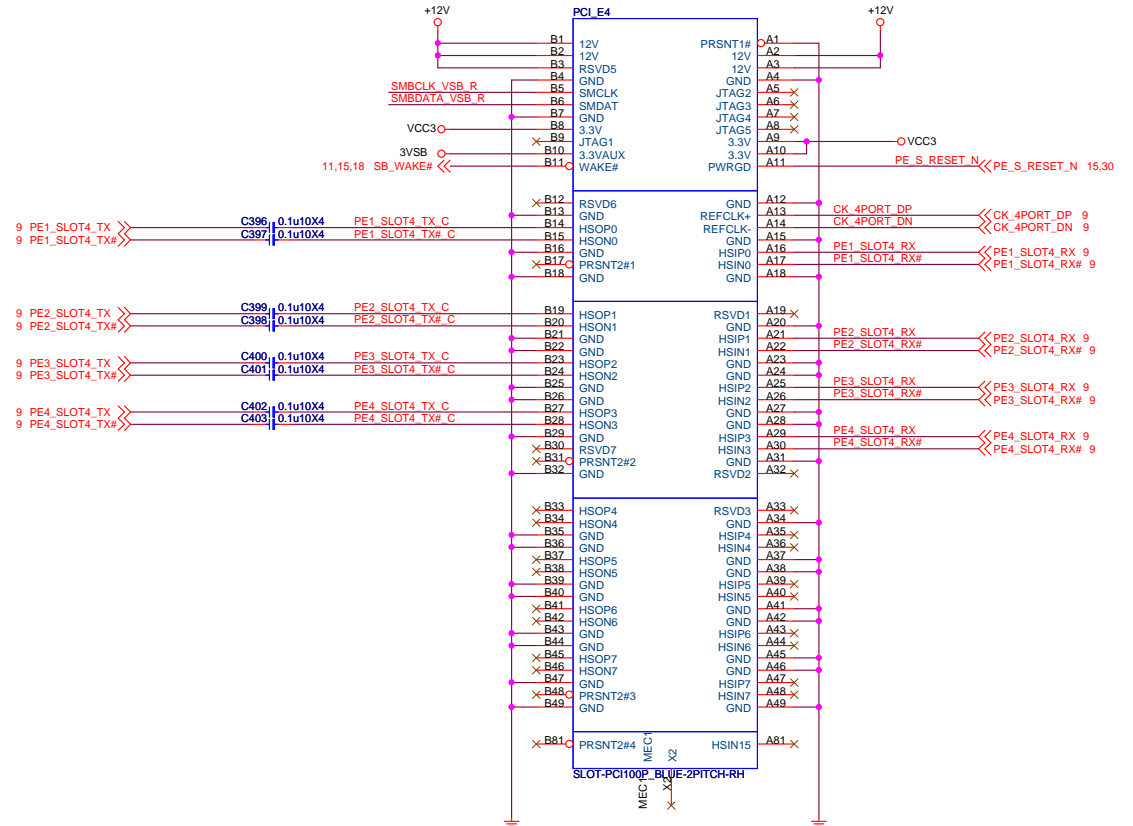




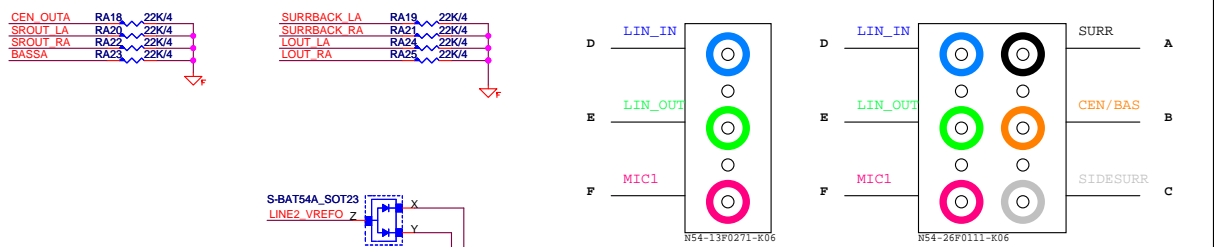
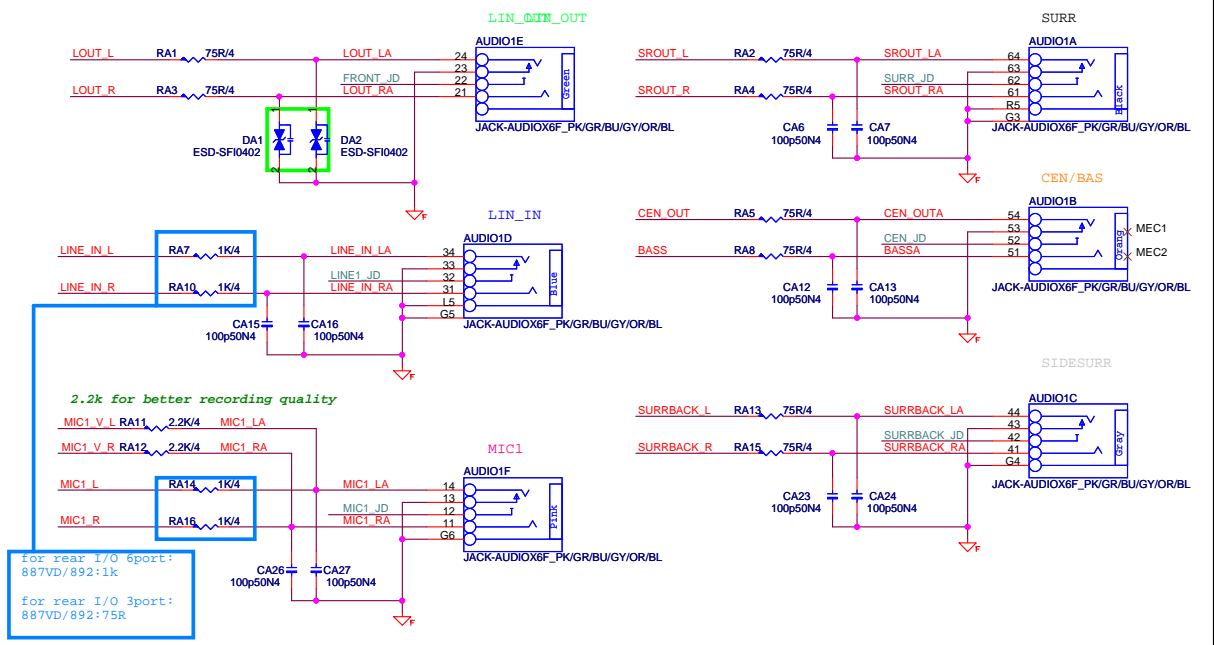
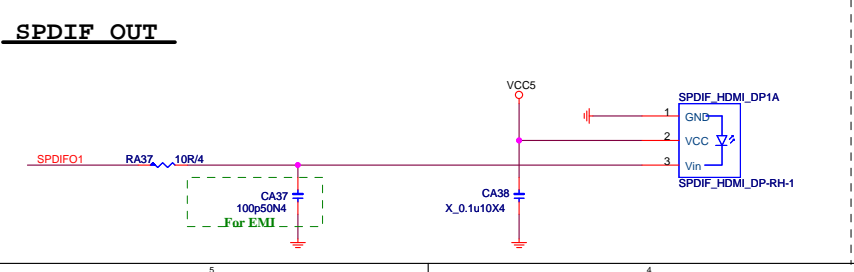
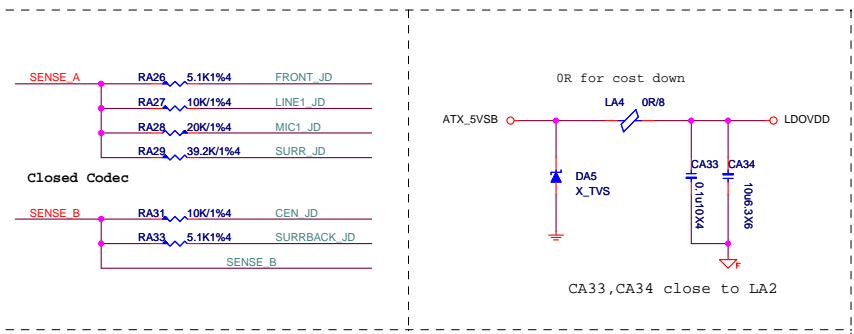
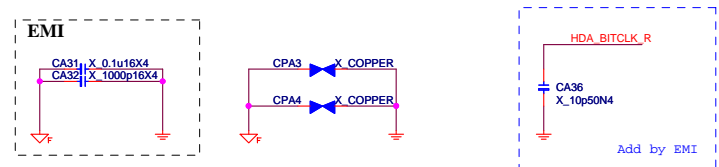
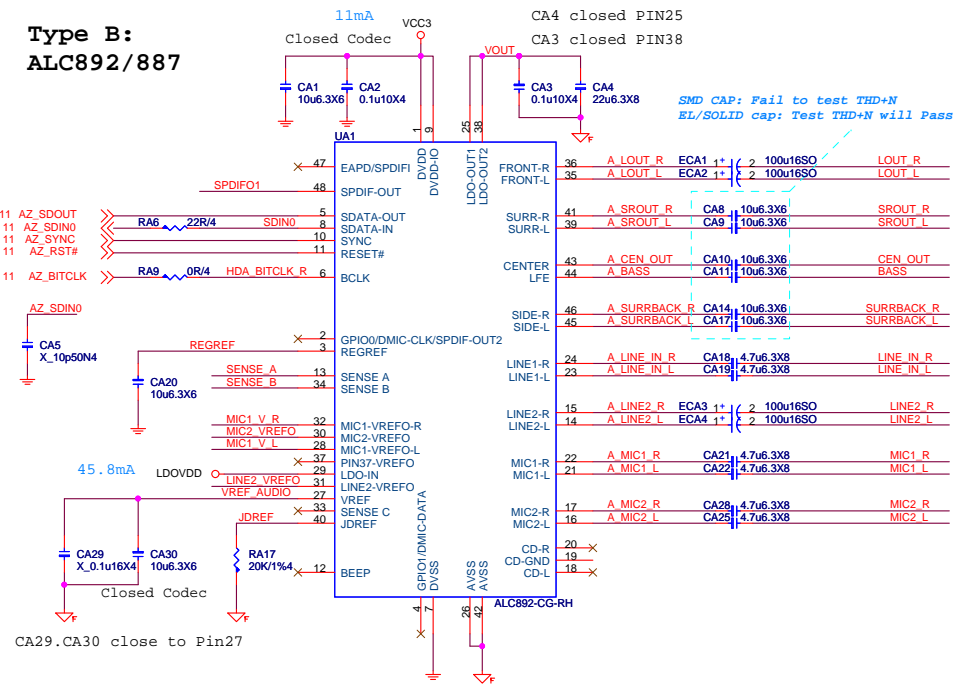
11,15 SMBCLK\_VSB\_R  
11,15 SMBDATA\_VSB\_R



## PCI Express X4 Slot

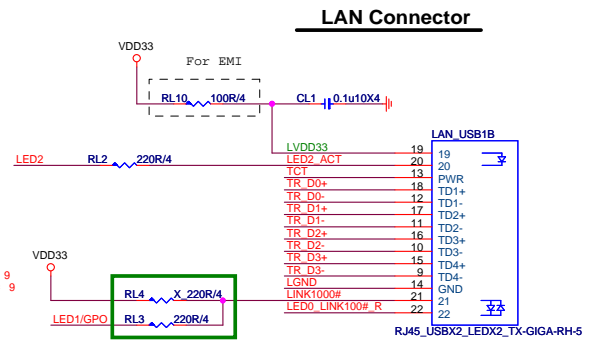
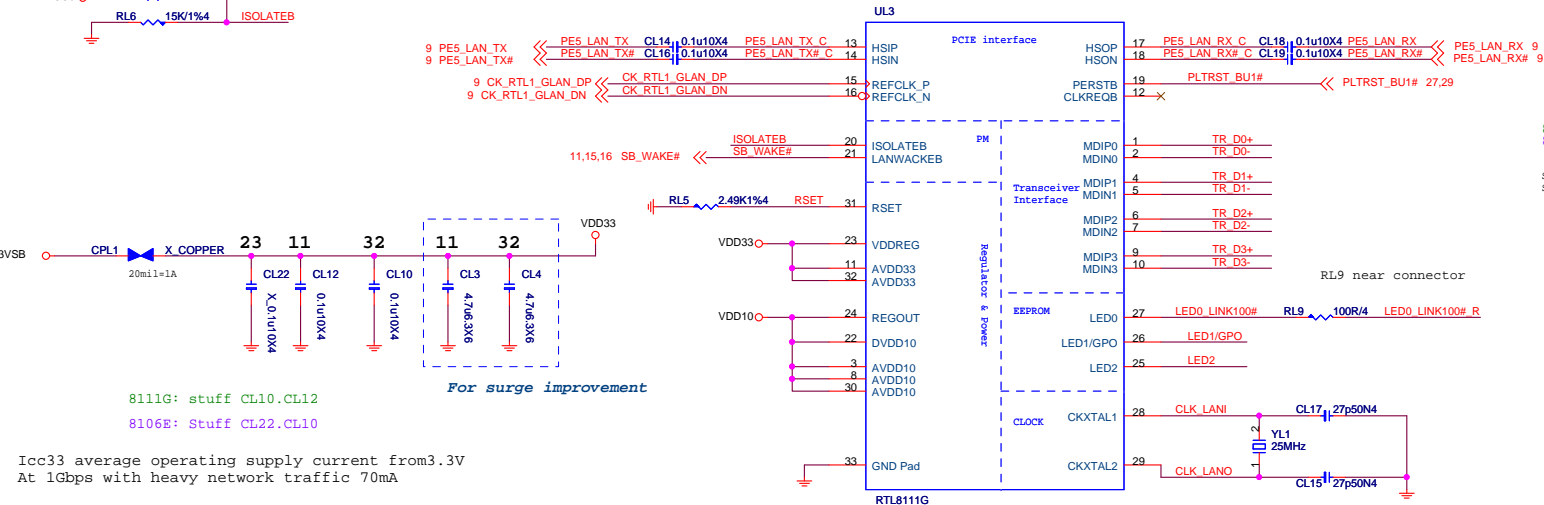
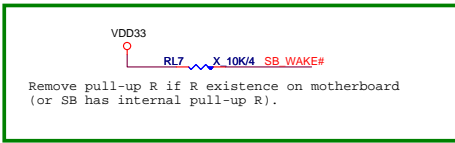


# Type B: ALC892/887



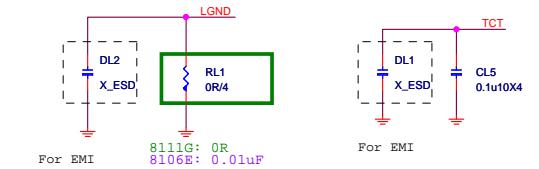
# RTL8111G Giga LAN

## RTL8106E 10/100M LAN

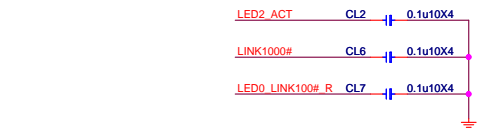


8111G: Keep RL6 and Remove RL5 for RTL8111G  
8106E: Keep RL5 and Remove RL6 for RTL8106E

Support R>= 249 ohm Resistor For Single Color LED.  
Support R>= 125 ohm Resistor For Dual Color LED.

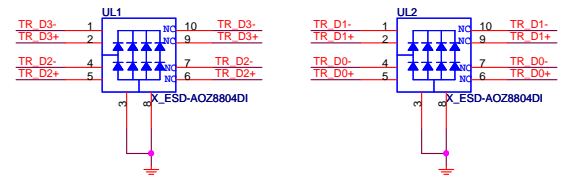


8111G: 0R  
8106E: 0.01uF



### Reserve ESD Protect

Change to 10 pin TVS by EMI



### 8106E POWER Consumption

	3.3V @ mA	mW
10 M Idle/TxRx	15/94	49.5/310.2
100 M Idle/TxRx	52/105	171.6/346.5
S0 ALDPS	4	13.2

### 8111G POWER Consumption

	3.3V @ mA	mW
10 M Idle/TxRx	17.15/116.7	56.6/385.1
100 M Idle/TxRx	71.45/129.5	235.8/427.4
Giga Idle/TxRx	179.1/243.9	591/804.9
ALDPS	6.41	21.15

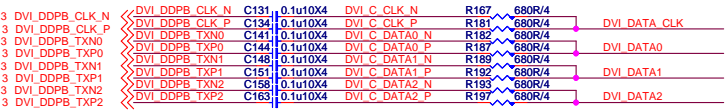


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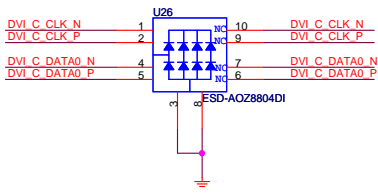
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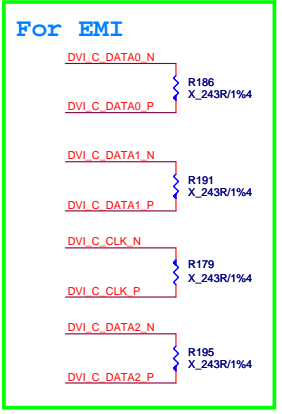
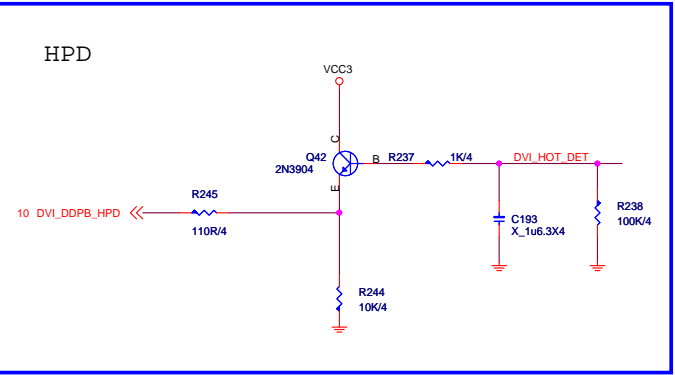
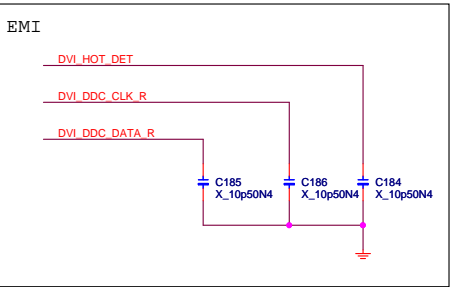
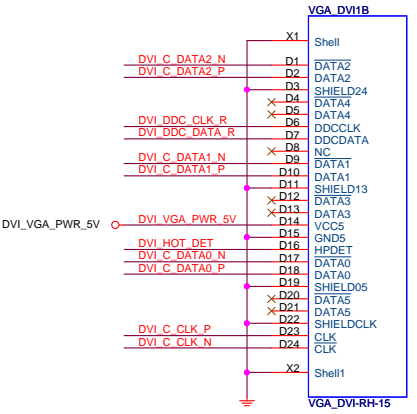
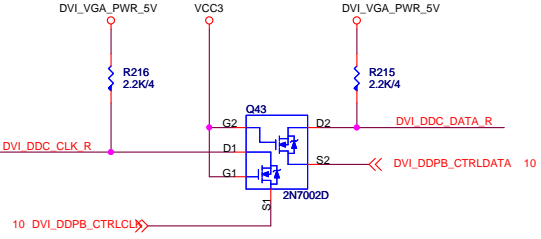
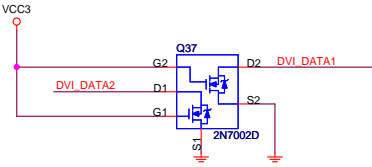
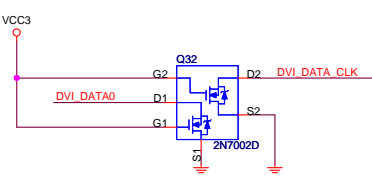
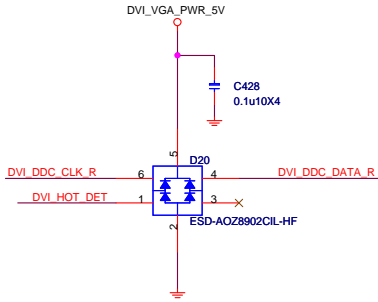
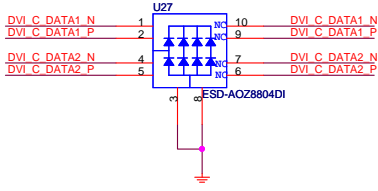
VGA: resolution of 2048x1536 pixels with 32-bit color at 75 Hz (4:3 QXGA)



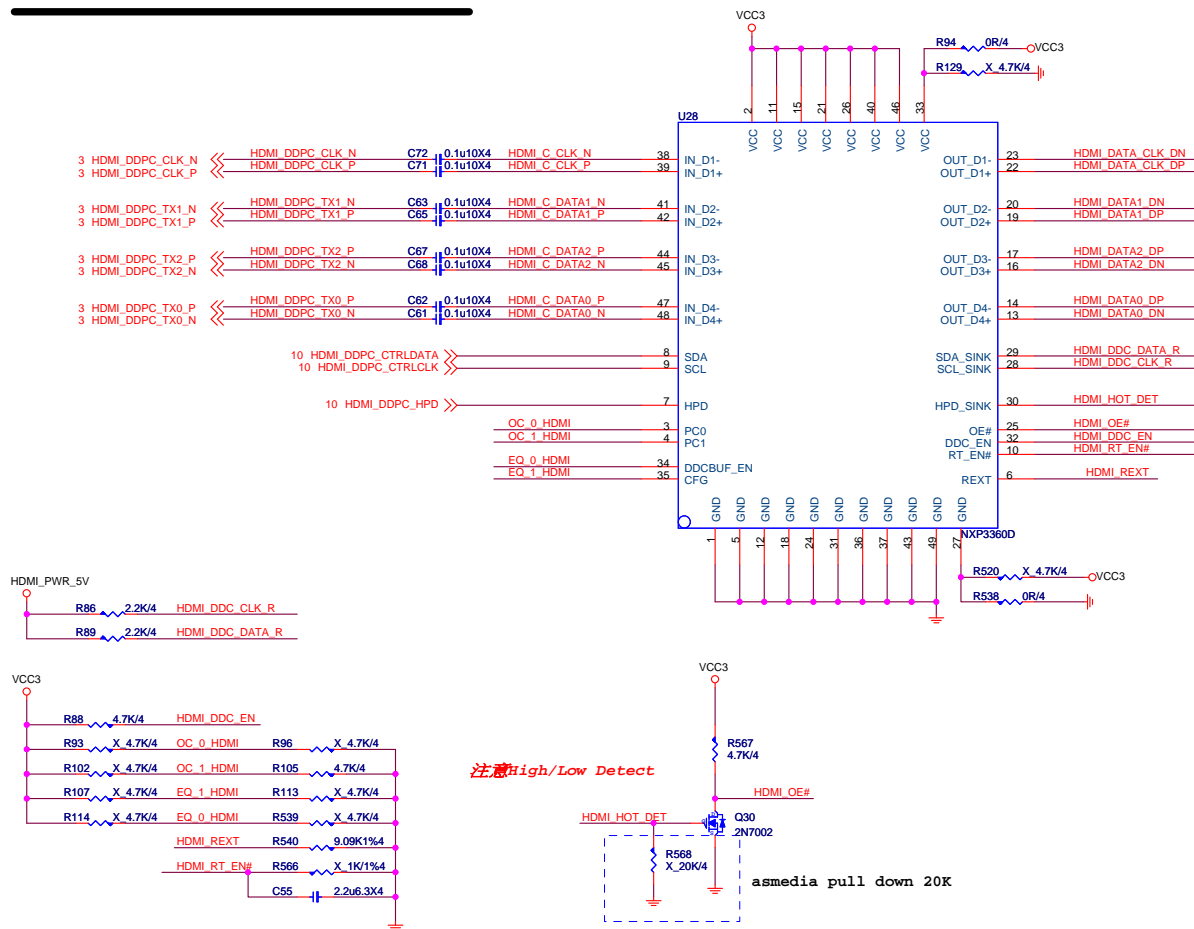
U26 AVL:D0G-05A050C-005  
D0G-06A050C-A68



U27 AVL:D0G-05A050C-005  
D0G-06A050C-A68



## HDMI level shifter



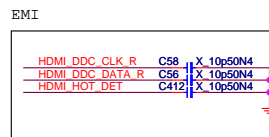
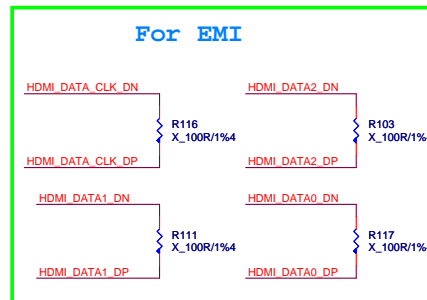
	"0"	"1"
DDC_EN	DDC level shifter disable	DDC level shifter enable
RT_EN#	Input 50 ohm termination resistor enable	the input termination ; resistors are set to high impedances
OE#	enable	the chip is power down and input termination resistors will be at high impedance.
HPD_SINK	disable	enable
DDCBUF_EN	For DDC level shifting configuration, please refer to Table.	
REXT		

**note**

- internal pull-up at ~500K ohm.
- internal pull-down at ~500K ohm.
- internal pull-down at ~500K ohm.
- internal pull-down at ~200K ohm;  
5V tolerant.
- internal pull-down at ~500K ohm.
- analog current generation.

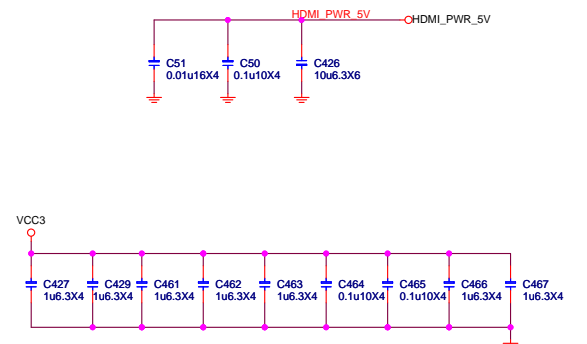
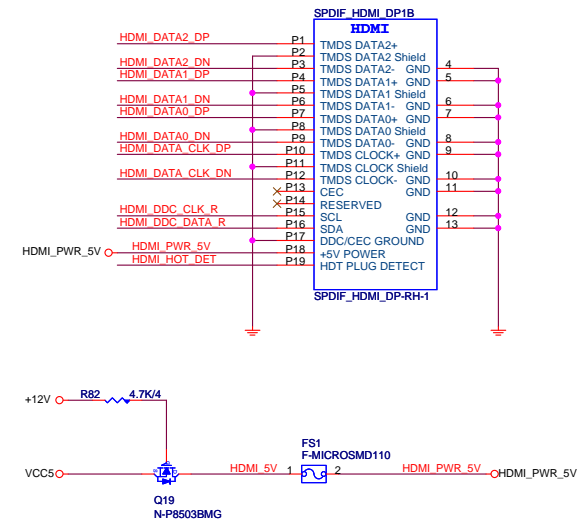
[DDC_EN, DDCBUF_EN, OE#]	DDC Passive Switch	DDC Active Buffer
1, 0, X	On	Off
1, 1, 0	Off	On
1, 1, 1	Off	Off

PC1, PC0		<b>note</b>
00	8 dB	internal pull-down at ~500K ohm.
01	4 dB	
10	12 dB	



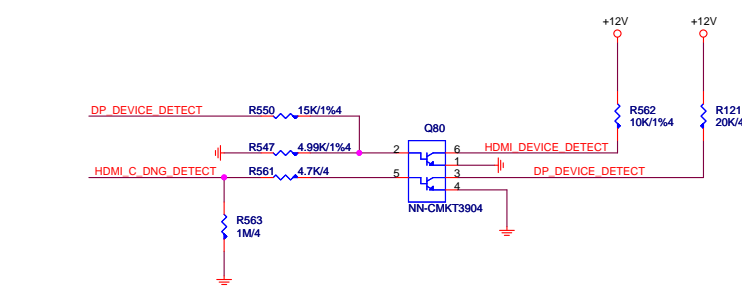
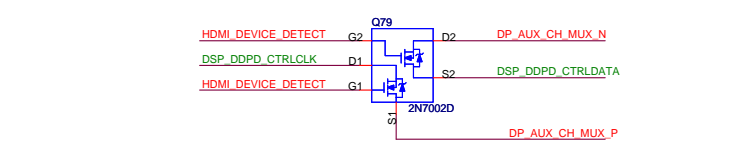
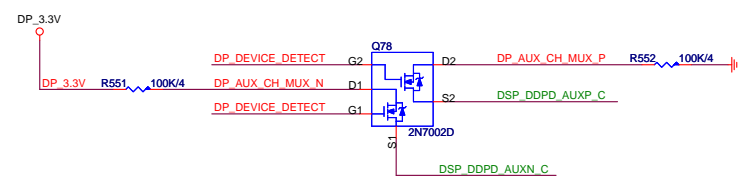
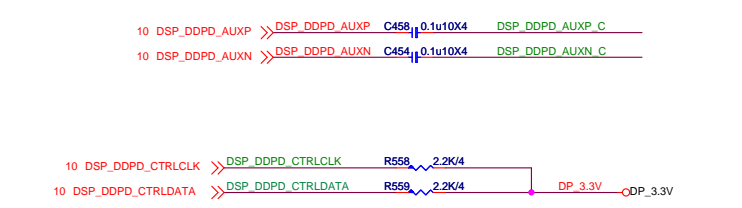
### Table 8-1. PCH PCI Express Tx/RX - HDMI Signal Mappings

Port	Digital Display Interface Differential Pairs	HDMI Signals	PCH Digital Display Interface Pins
Port B	DDSP_B_TX0_ON	TMDSB_DATA2#	DDPB_0N
	DDSP_B_TX0_DP	TMDSB_DATA2	DDPB_0P
	DDSP_B_TX1_ON	TMDSB_DATA1#	DDPB_1N
	DDSP_B_TX1_DP	TMDSB_DATA1	DDPB_1P
	DDSP_B_TX2_ON	TMDSB_DATA0#	DDPB_2N
	DDSP_B_TX2_DP	TMDSB_DATA0	DDPB_2P
	DDSP_B_TX3_DN	TMDSB_CLK#	DDPB_3N
	DDSP_B_TX3_DP	TMDSB_CLK	DDPB_3P
	DDPB_HPD	DDSP_B_HPD0	Hot plug detect used by HDMI Port B.
	SDVO_CTRLCLK	HDMIb_CTRL_CLK	HDMI DDC lines for Port B
SDVO_CTRLDATA	HDMIb_CTRL_DATA		

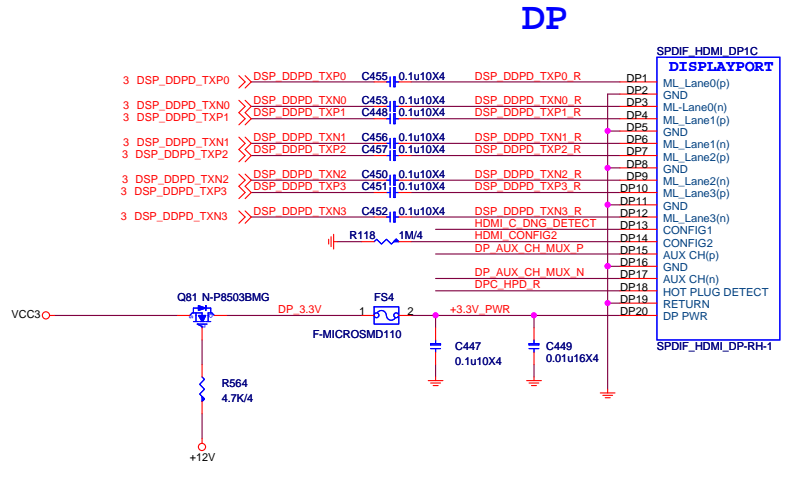
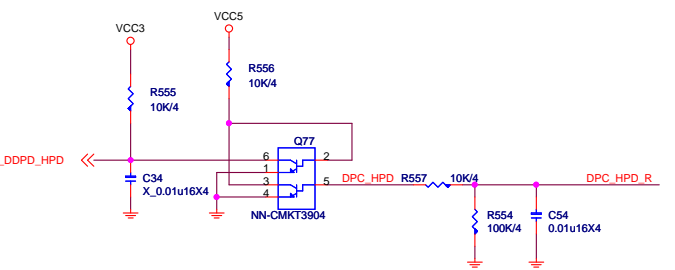
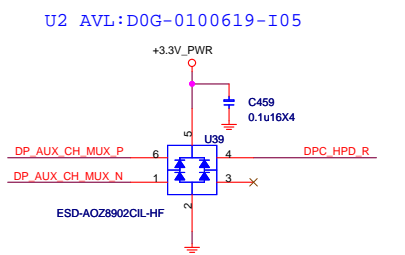
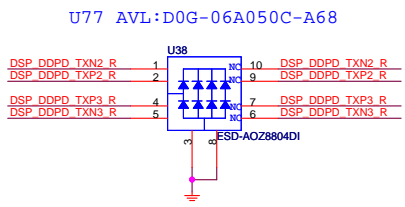
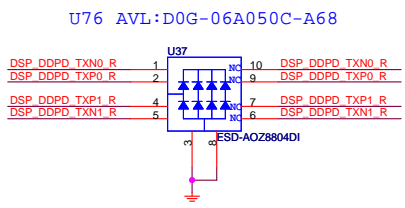


<b>MICRO-STAR INT'L CO.,LTD</b>			
<b>MS-7823</b>			
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	DP	HDMI
HDMI_C_DNG_DETECT	L	H
DP_DEVICE_DETECT	H	L
HDMI_DEVICE_DETECT	L	H



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**MS-7823**

Size: Custom

Document Description: Display port connector

Date: Monday, March 25, 2013

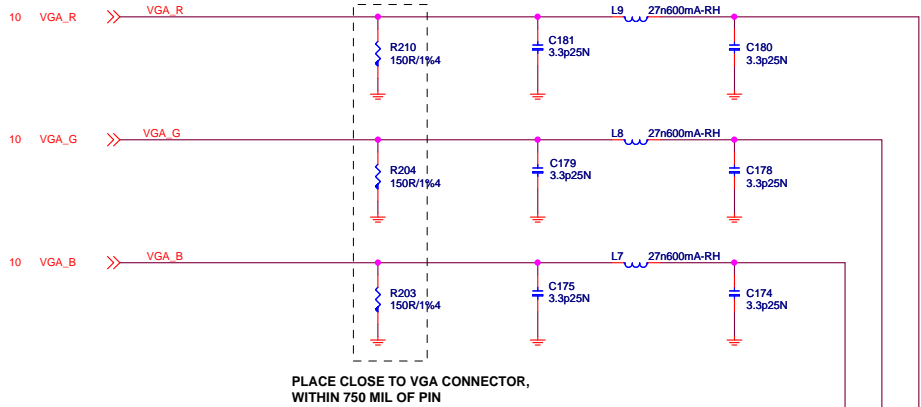
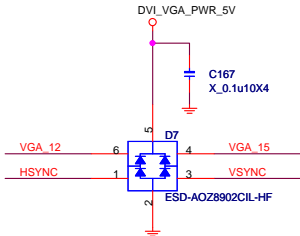
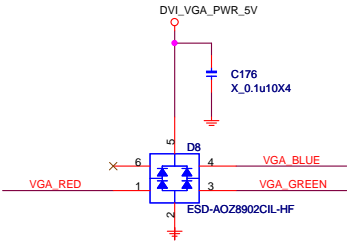
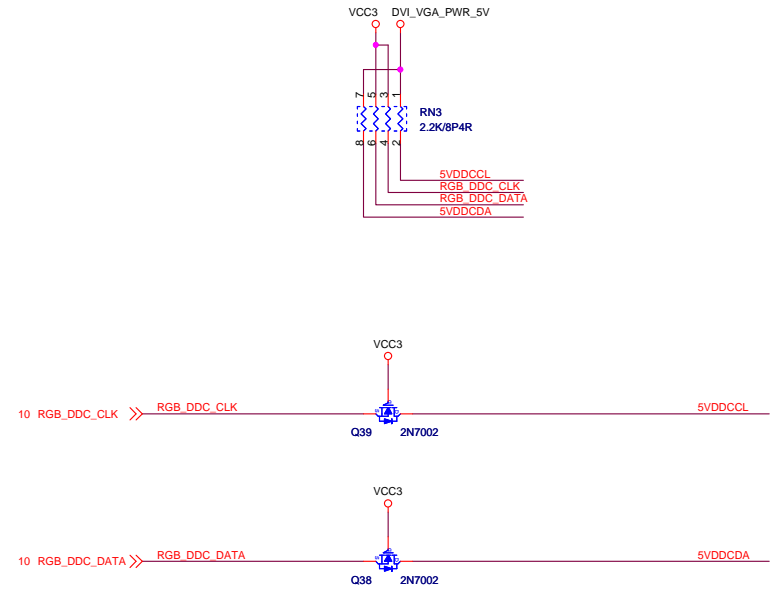
Rev: 11

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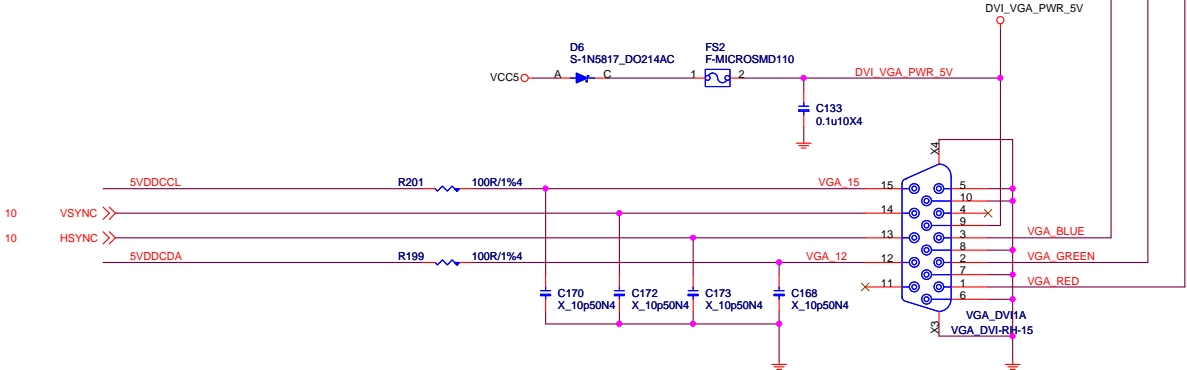
D-Sub

VGA: resolution of 2048x1536 pixels with 32-bit color at 75 Hz (4:3 QXGA)

Level shift

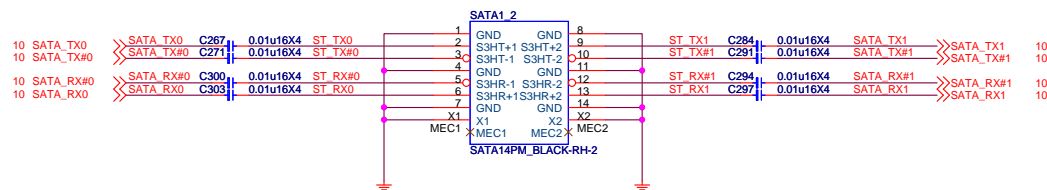


PLACE CLOSE TO VGA CONNECTOR,  
WITHIN 750 MIL OF PIN



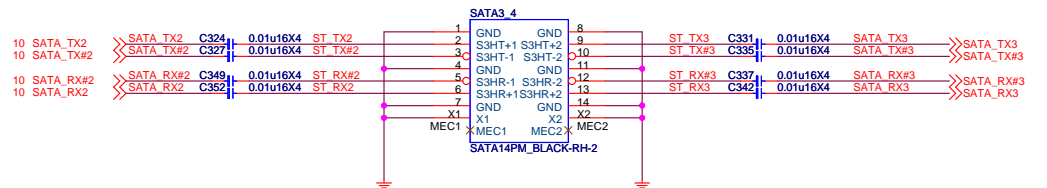
### SATA 6G PORT 0,1

3.0 Black



### SATA 3G PORT 2,3

3.0 Black

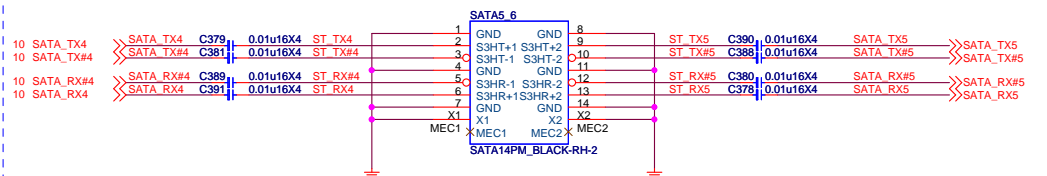


### SATA 3G PORT 4,5

Change 90 by PM

3.0 Black

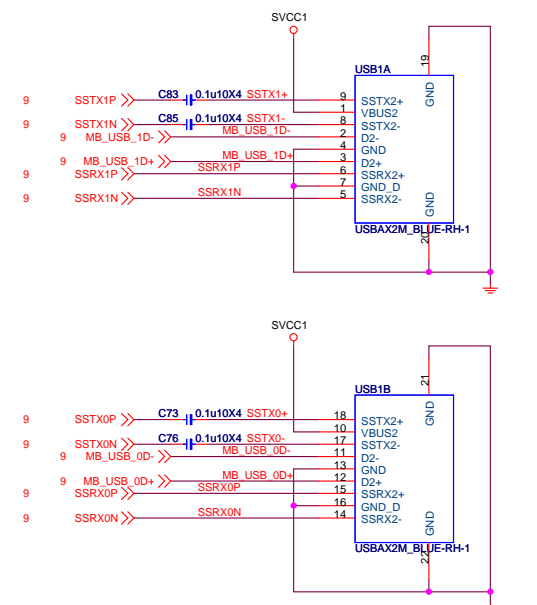
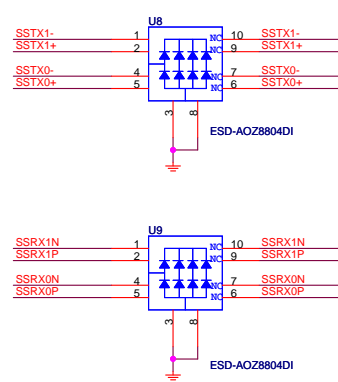
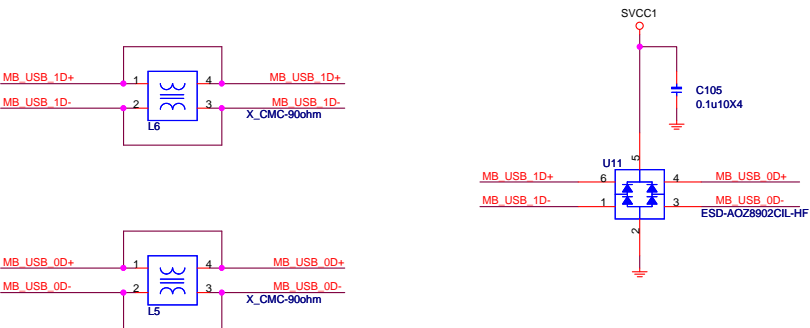
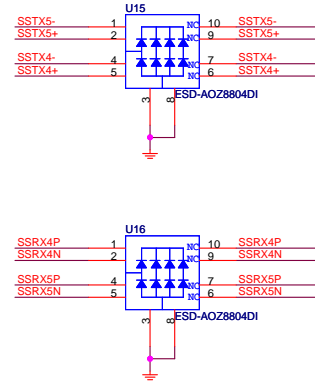
Z87,H87 chip support SATA3.0  
B85 chip support SATA2.0



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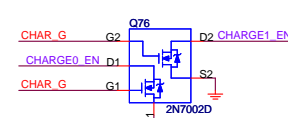
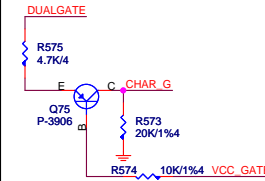
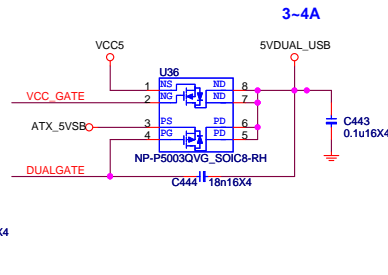
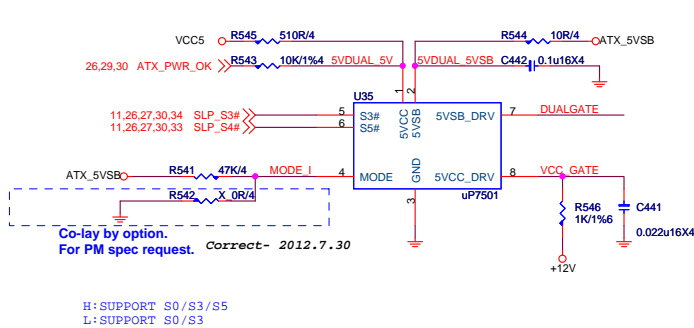
Size	Document Description	Rev
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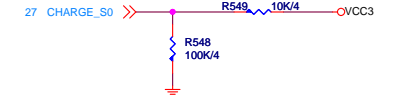
MS-7823

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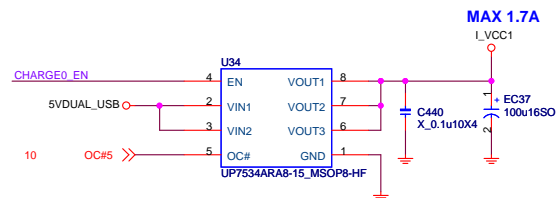
## 5VDUAL\_USB - uP7501



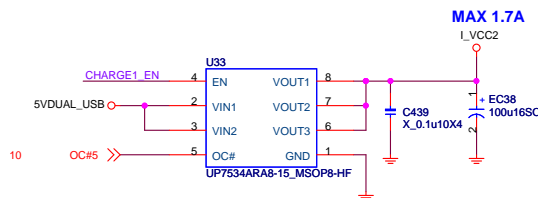
F71868 GPIO12  
NCT6779D GPIO24  
F71889 GPIO25



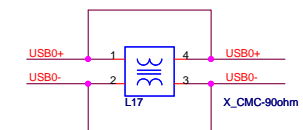
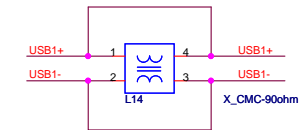
## USB POWER PORT 0 For USB Charging



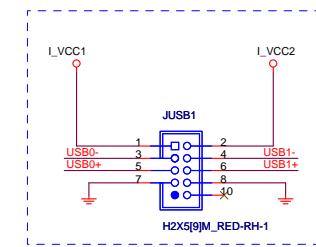
## USB POWER PORT 1 For USB Charging



## FRONT USB PORT 0,1

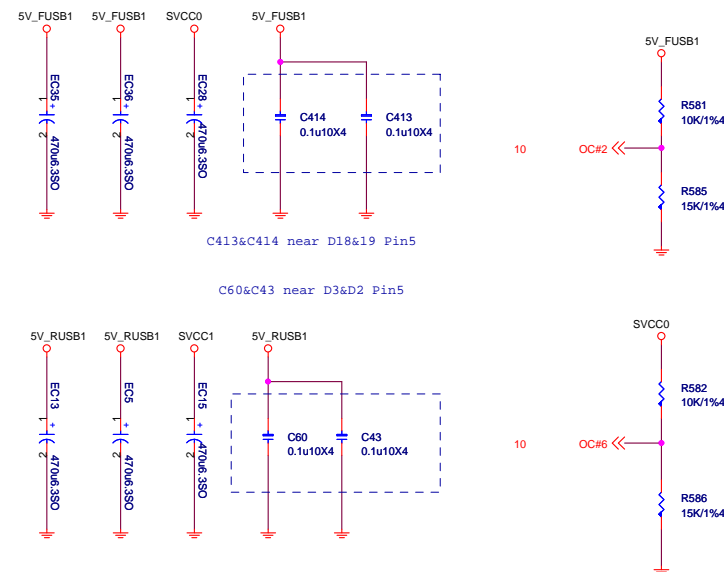
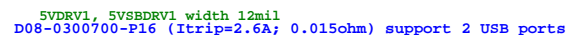


SLG55583A has internal ESD diode.

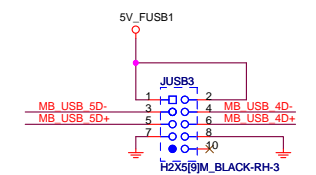
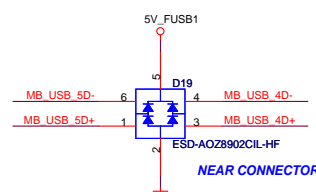
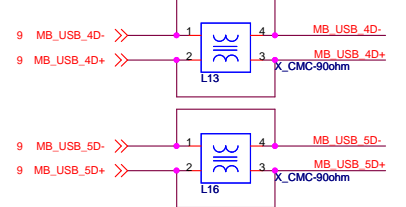


Please name the pin header JUSB1.

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**FRONT USB PORT 4,5(OC2#)**



**MICRO-STAR INT'L CO.,LTD**

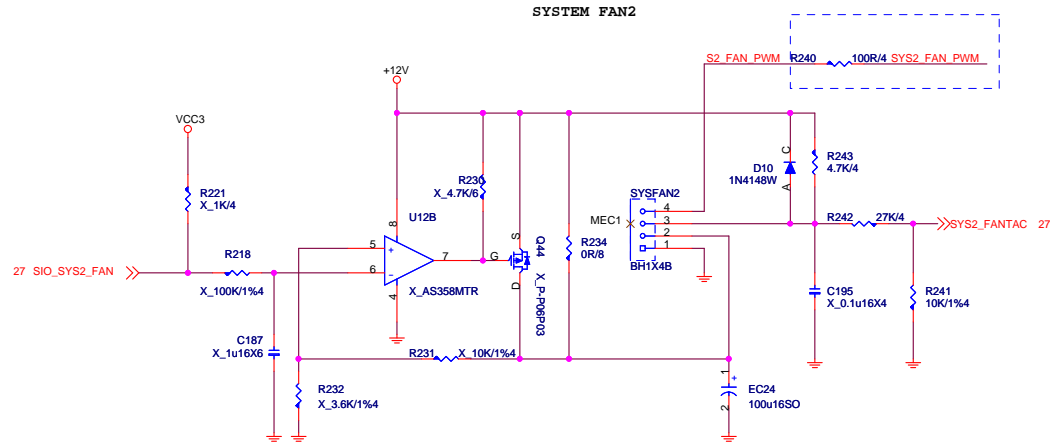
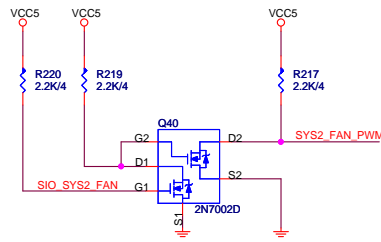
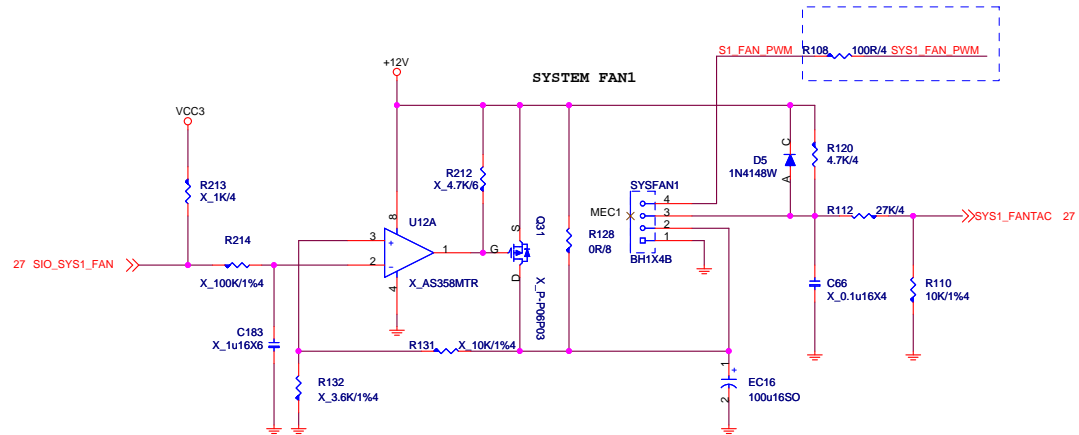
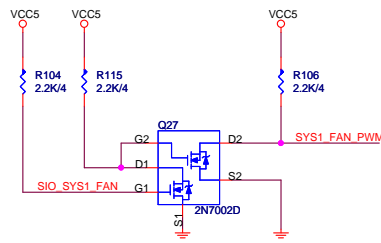
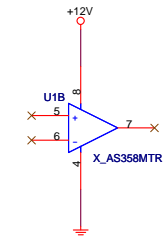
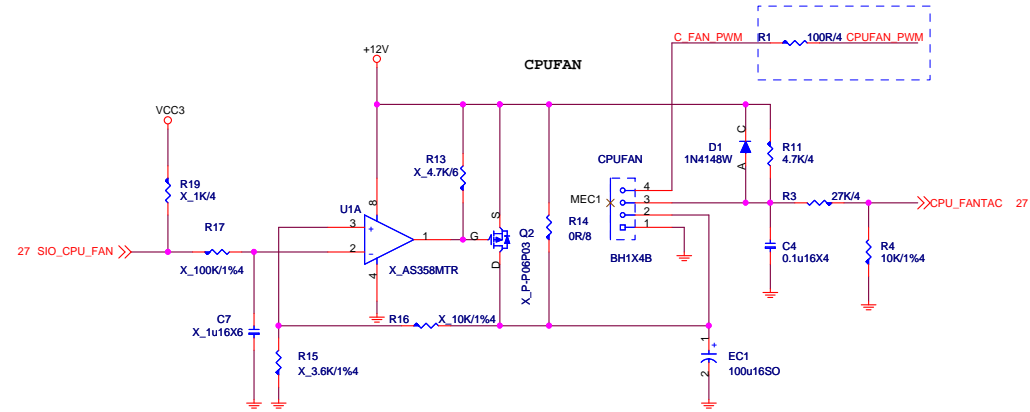
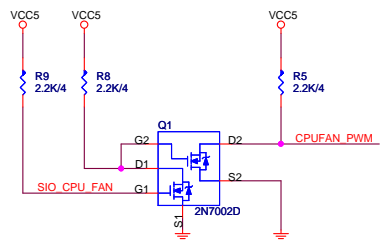
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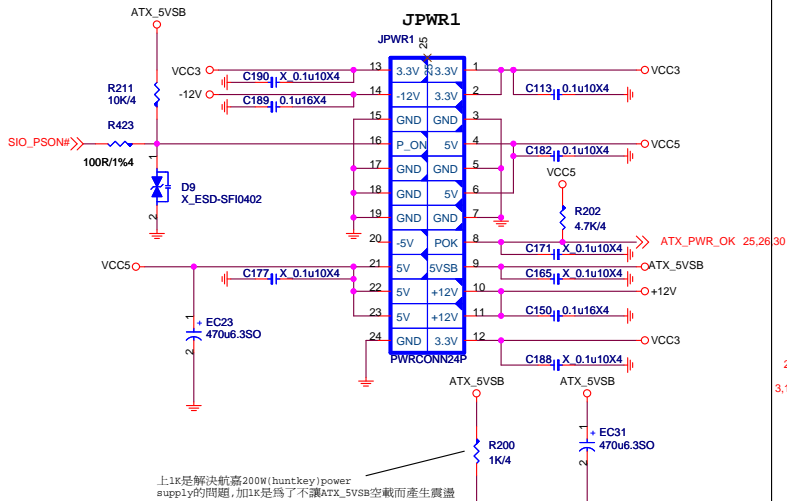




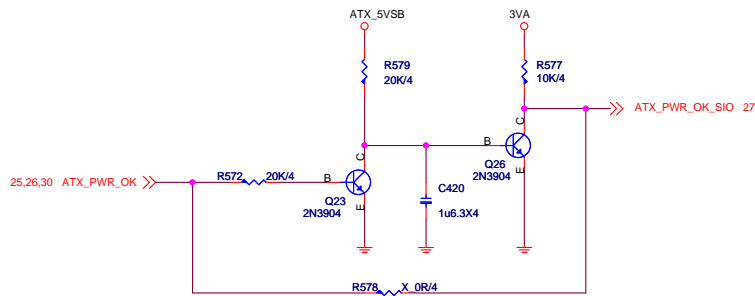
# FAN-COUNTROL CIRCUIT



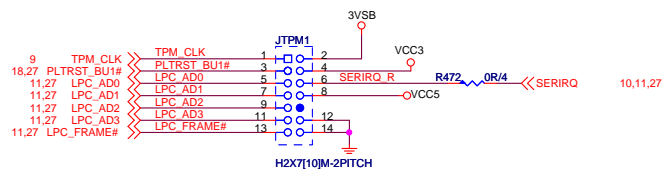
## ATX POWER CONNECTOR



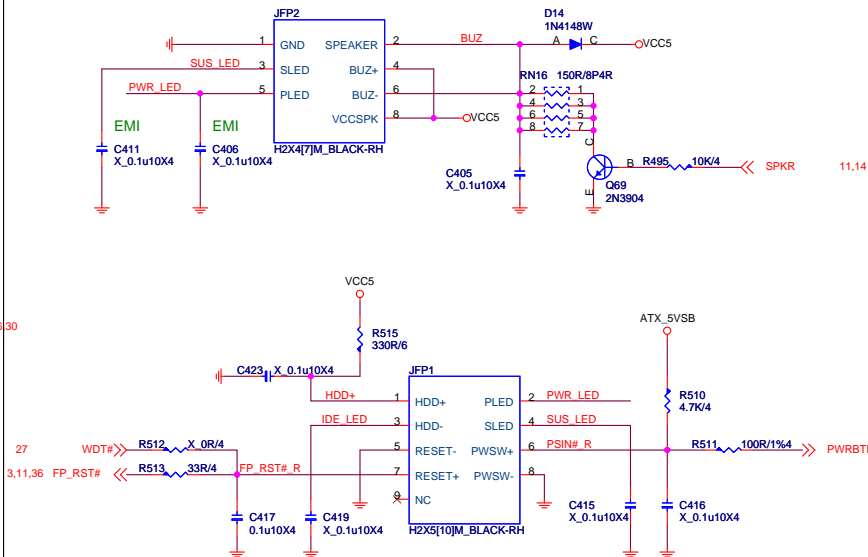
5VCC leakage from ATXPGD. (NCT6779 PIN80)



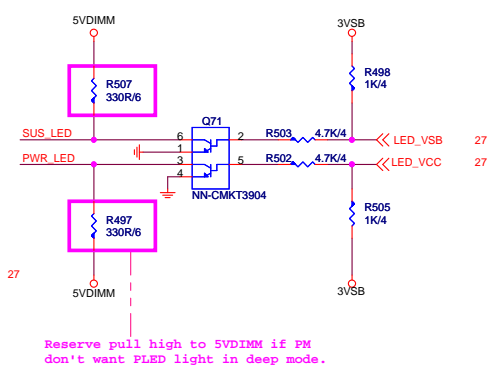
## TPM



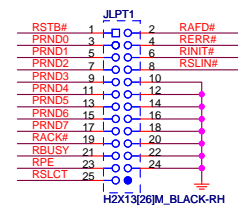
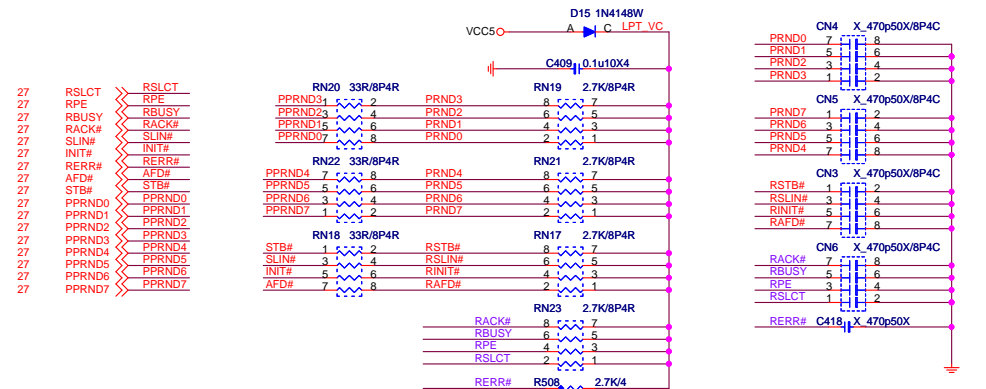
## FRONT PANNEL



## LED ( for Fintek 71869)

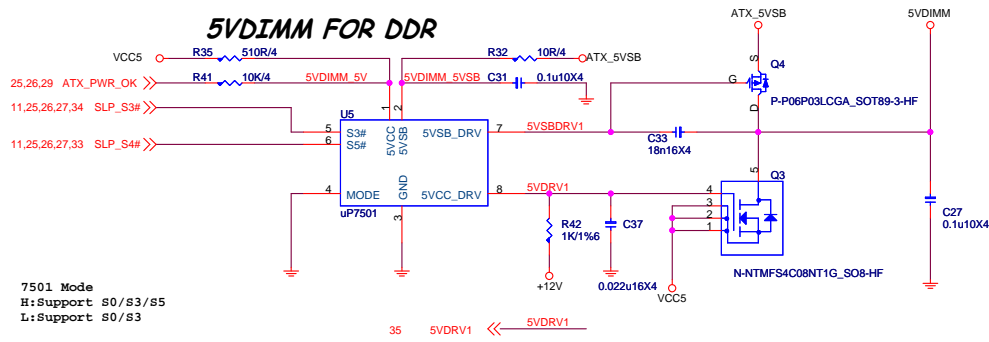


## PARALLAL PORT

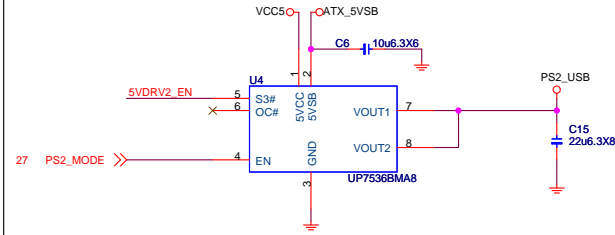


N31-2131151-H06 : 2.0mm  
N31-2131131-H06 : 2.54mm

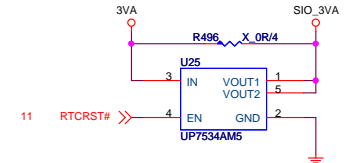
## 5VDDIMM FOR DDR



## PS2 Power

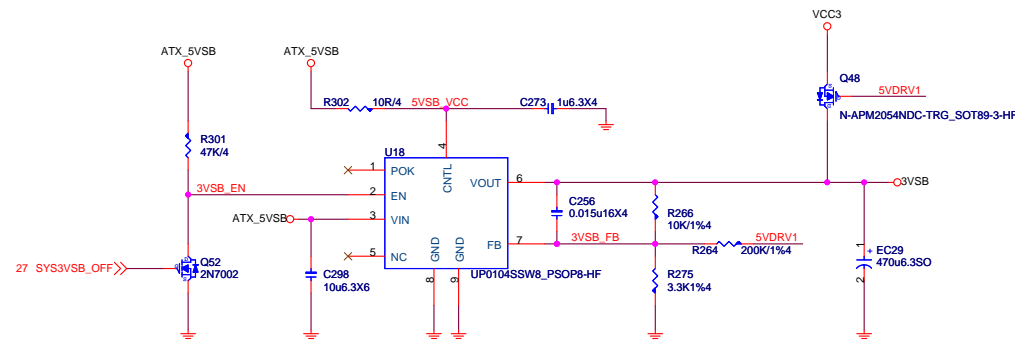


## 隔離PCH&SIO的3VA

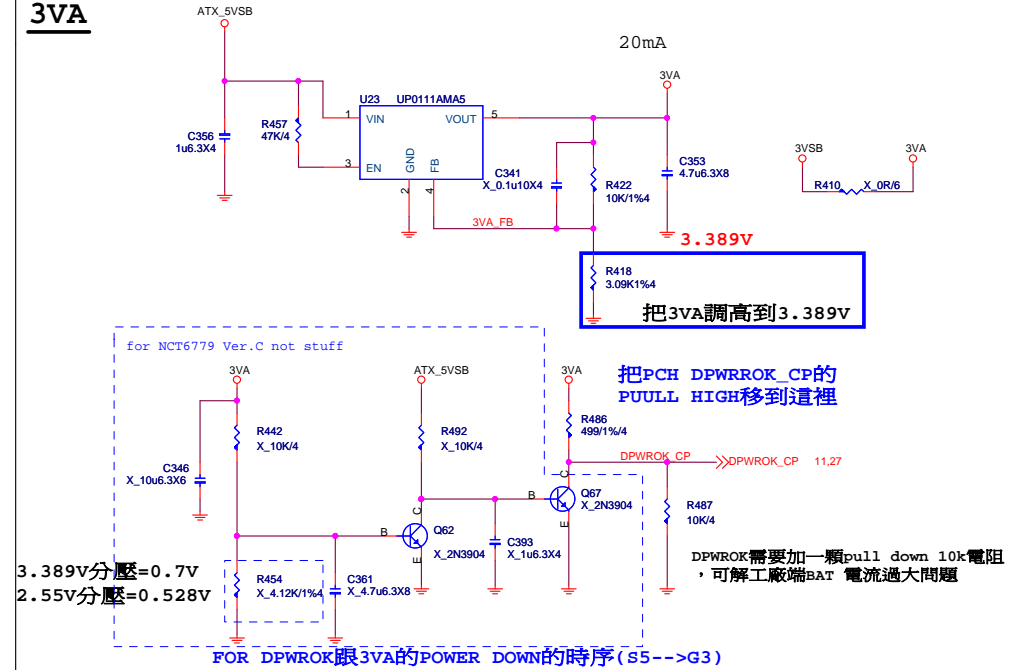


## 3VSB

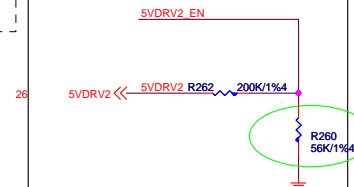
$0.216 + 0.2 + 1.5 + 0.67 = 2.586A$   
PCH: 216mA  
LAN: 200mA  
PCIE slot: 375mA x4  
up0104 ME Power: 0.67A



## 3VA

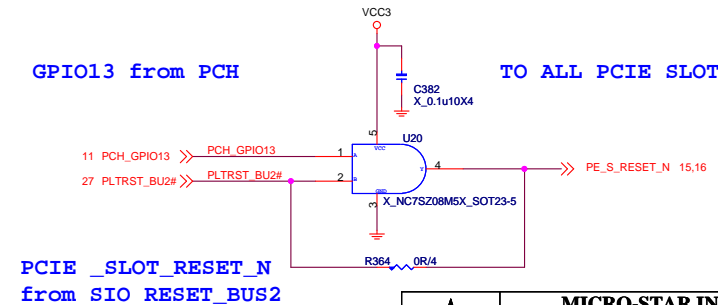


## USB MODE



## GPIO13 from PCH

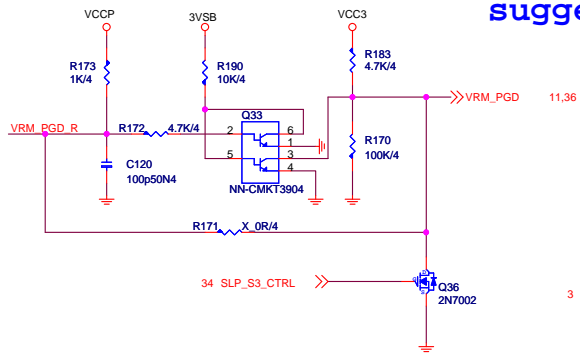
## TO ALL PCIE SLOT RESET#



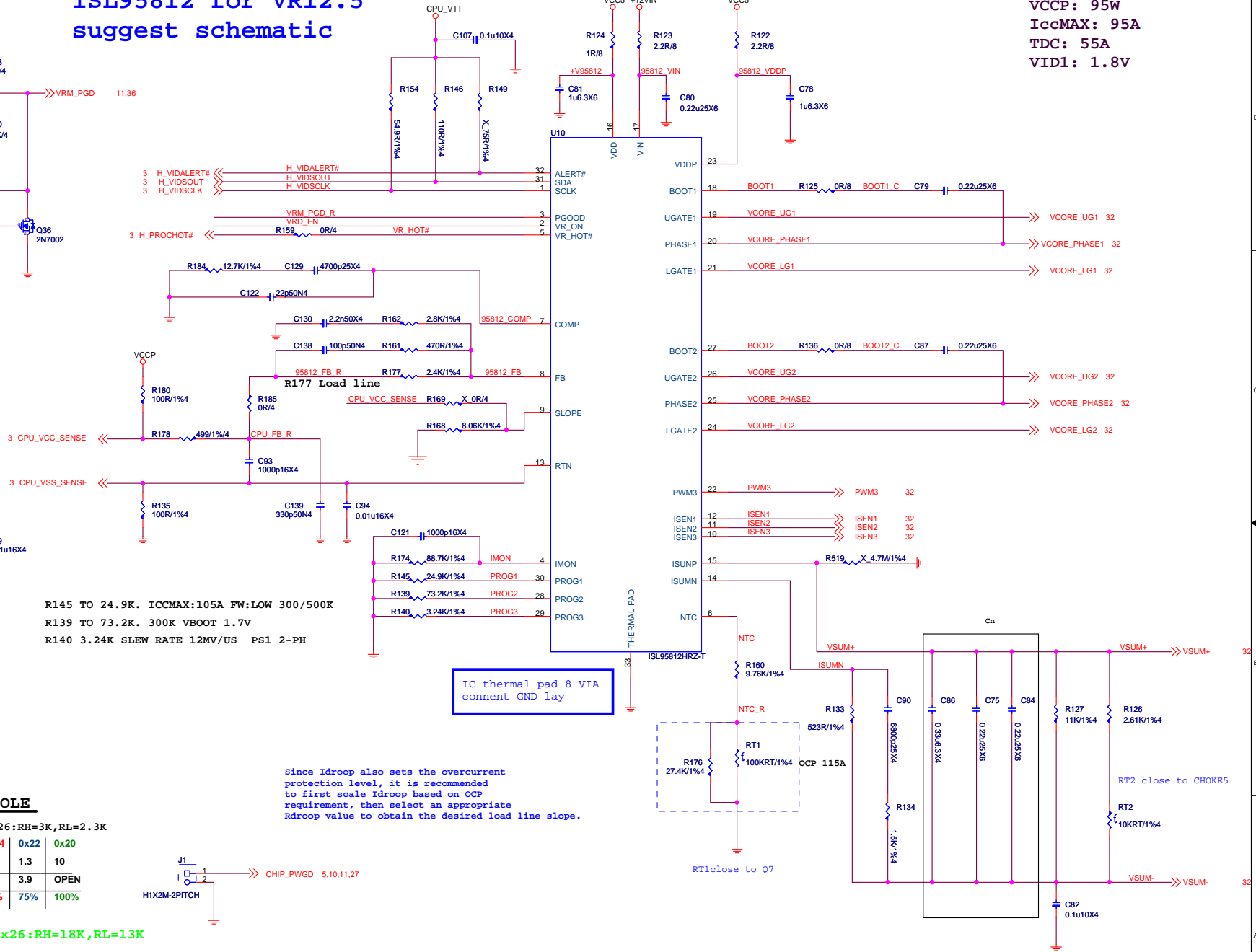
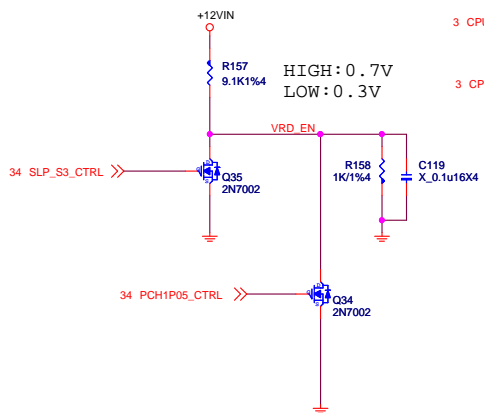
MICRO-STAR INT'L CO.,LTD		
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ISL95812 for VR12.5  
suggest schematic

VCCP: 95W  
IccMAX: 95A  
TDC: 55A  
VID1: 1.8V



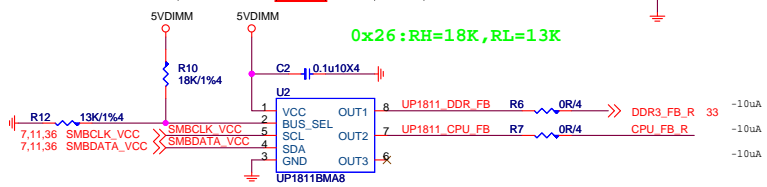
VCORE power on by s3 and 12v



## UPI VOLTAGE CONSOLE

	0x26: RH=3K, RL=2.3K					
ADDRESS	0x2A	0x28	0x26	0x24	0x22	0x20
RH (KOhm)	OPEN	3.9	3	2.2	1.3	10
RL (KOhm)	10	1.3	2.3	3	3.9	OPEN
BUS_SEL	0%	25%	40%	60%	75%	100%

0x26:RH=18K,RL=13K



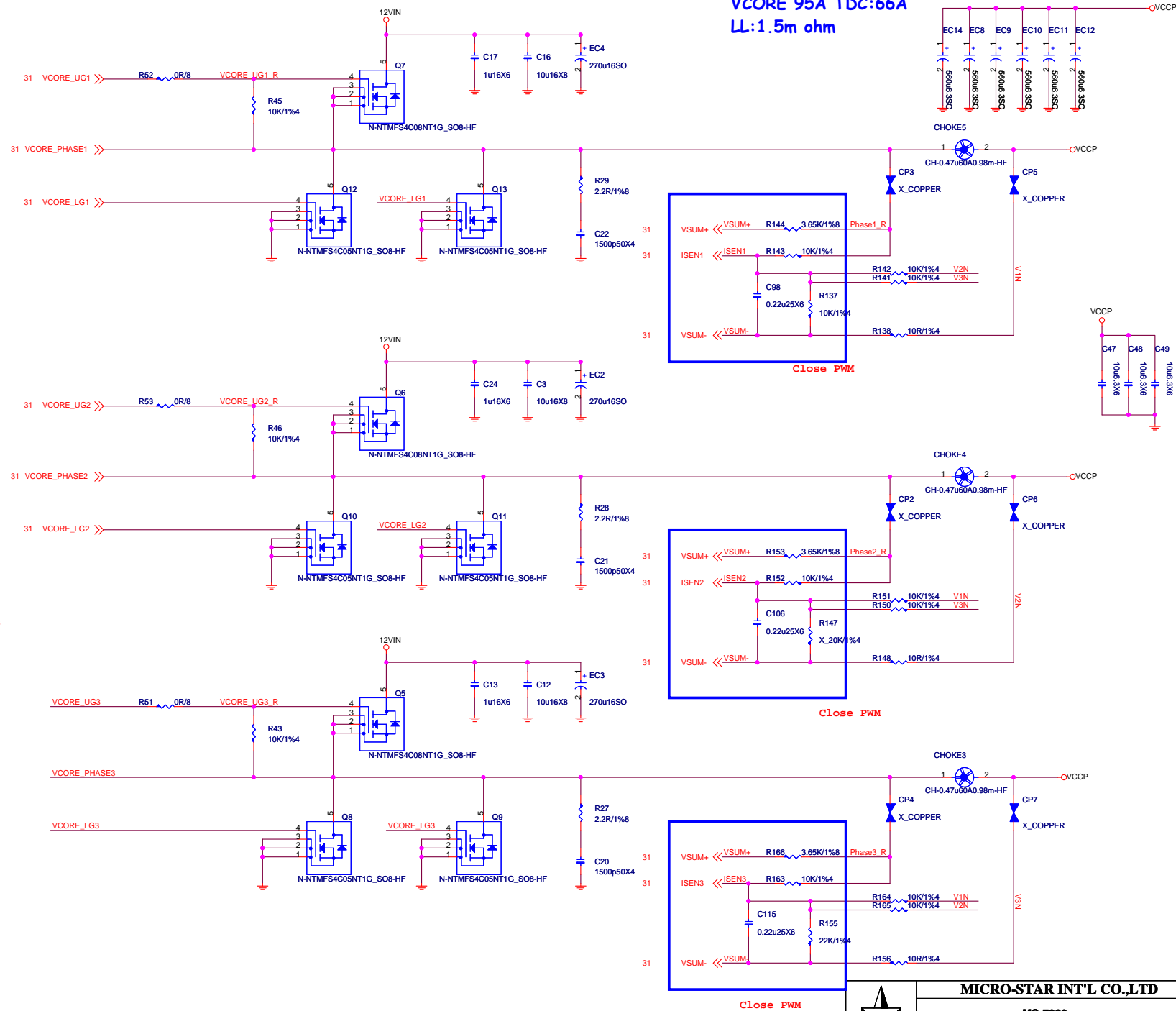
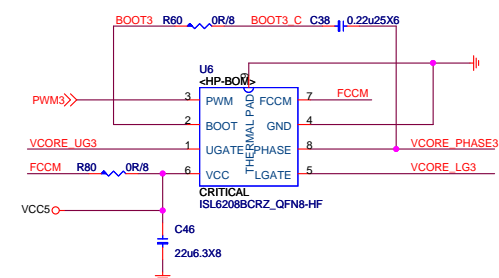
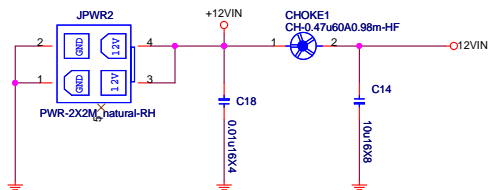
**MICRO-STAR INT'L CO.,LTD**

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OUTPUT CURRENT: ICCMAX 95A  
 Irms = 15.76A  
 Input Cap 5.08A\*3= 15.24A

VCORE 95A TDC:66A  
 LL:1.5m ohm



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# DDR Power:1.5V

DDR3\_1.5V 4.2A+12A+1.115A+5.921A=23.236A

4.2A FOR CPU

12A FOR 4DIMM

1.115A FOR VTT\_DDR

5.921A FOR PCH

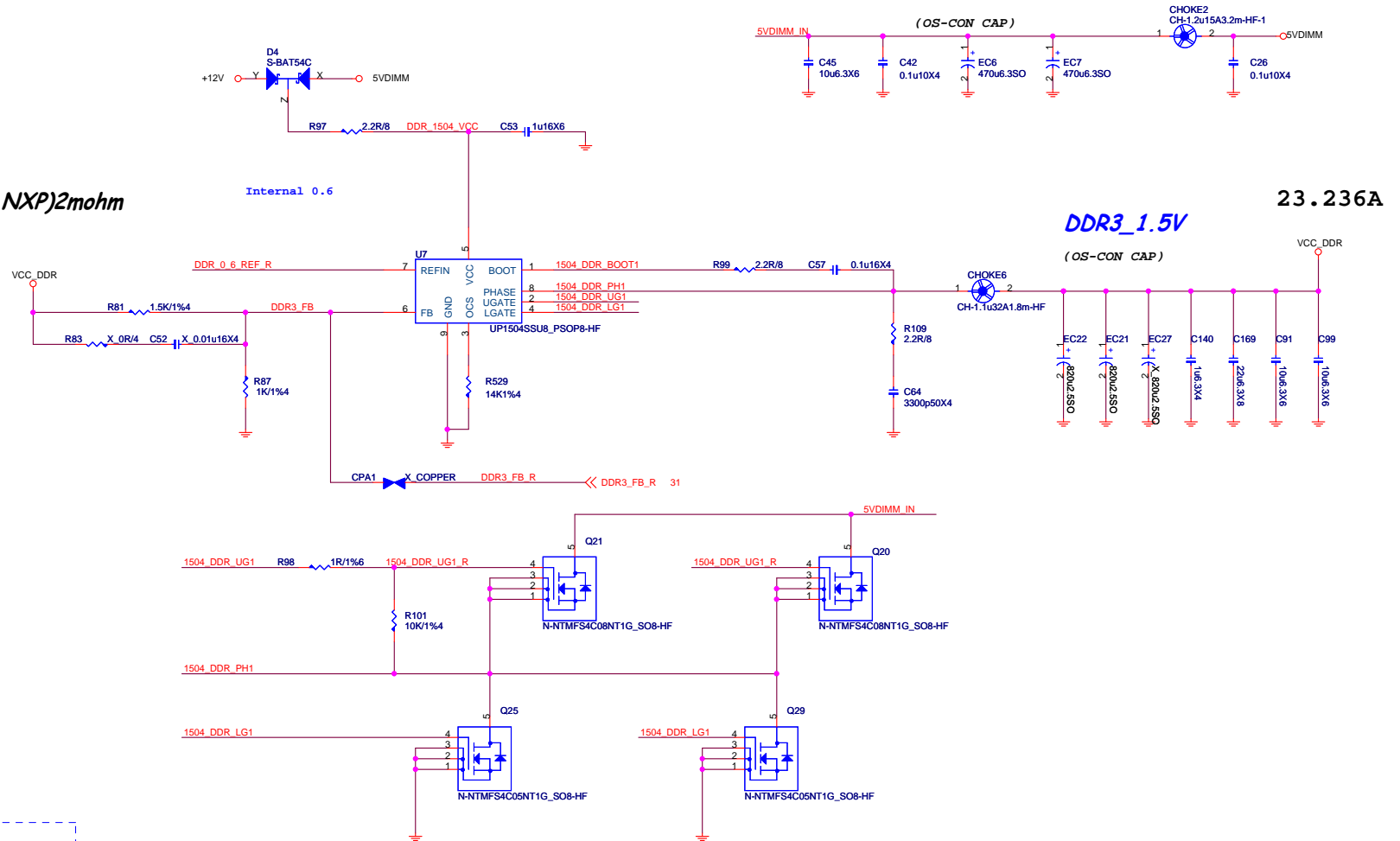
OCP 23.236A\*1.5=34.845A

OCP=[20uA\*Rocs(R320)]/4\*Rdson(Low side NXP)2mohm

R529=14K ohm

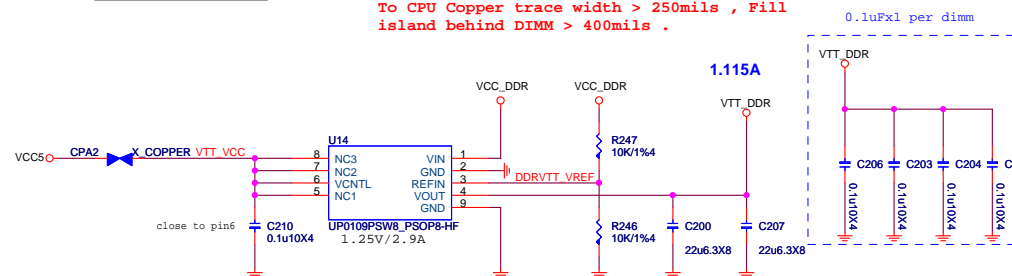
Iripple=10.64807288A

4.7\*2\*1=9.4A



## DDR VTT Power

To CPU Copper trace width > 250mils , Fill island behind DIMM > 400mils .



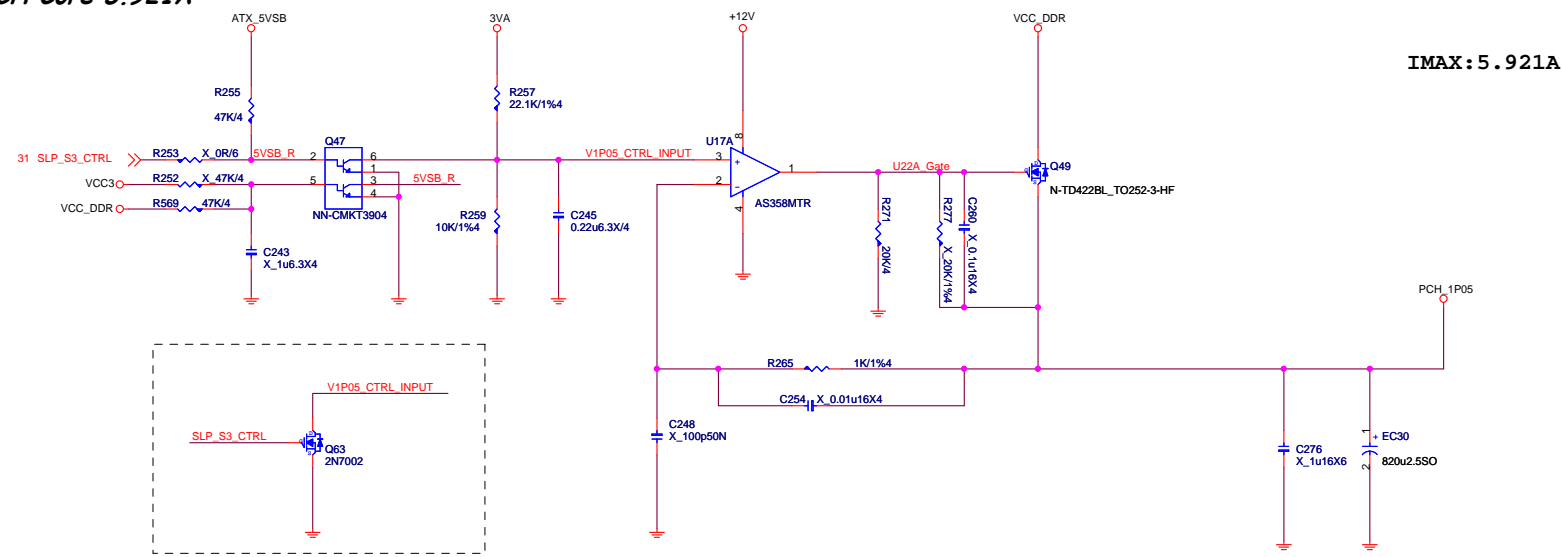
MICRO-STAR INT'L CO.,LTD

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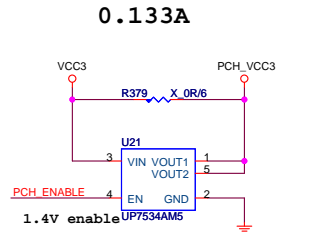
Size	Document Description	Rev
Custom	DDR Power - UP1504S 2-Phase MOS	11
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P.S. Only for meet Intel power down sequence.

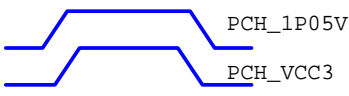
PCH Power:1.05V  
PCH Core 5.921A



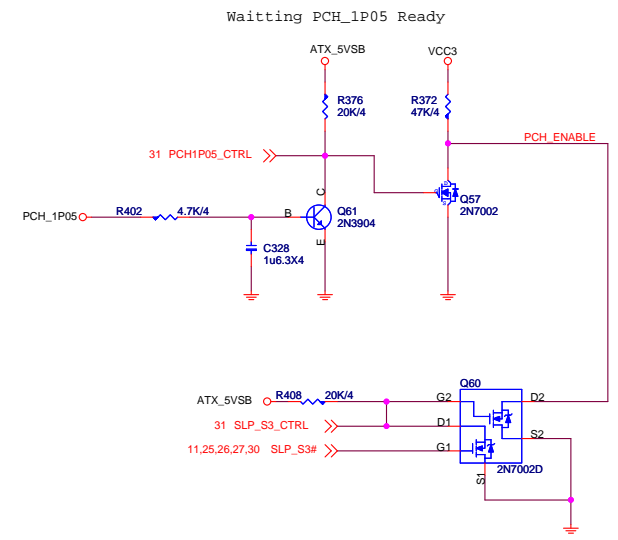
PCH Power:3.3V



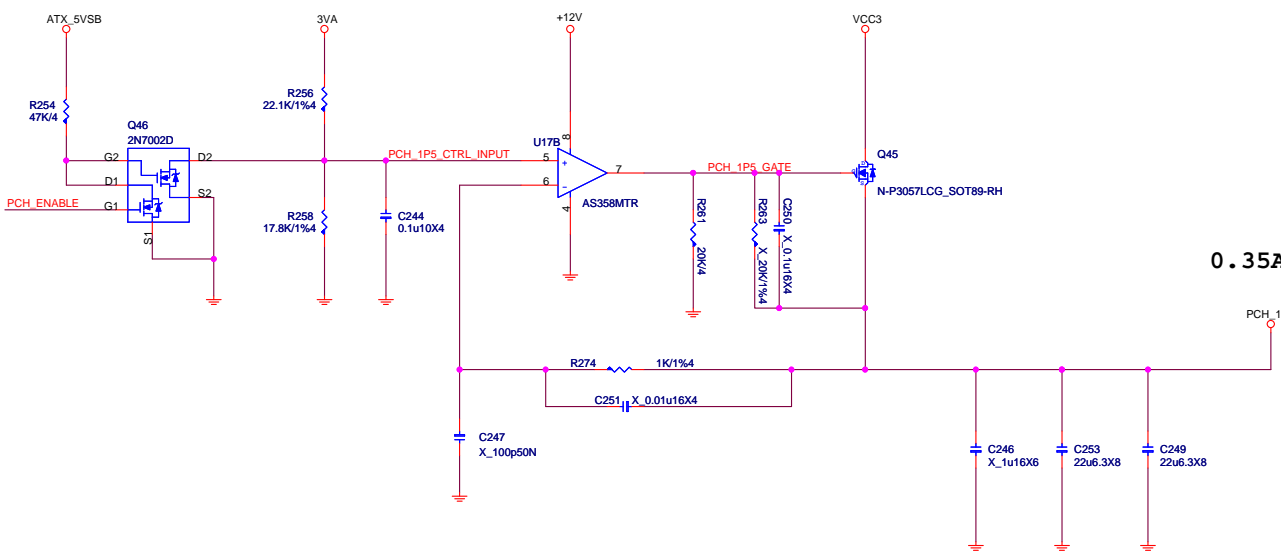
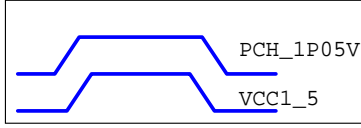
VCC1\_5\_CTRL\_INPUT:  
0:1P05V low or S3 low  
1:1P05V HIGH and S3 HIGH



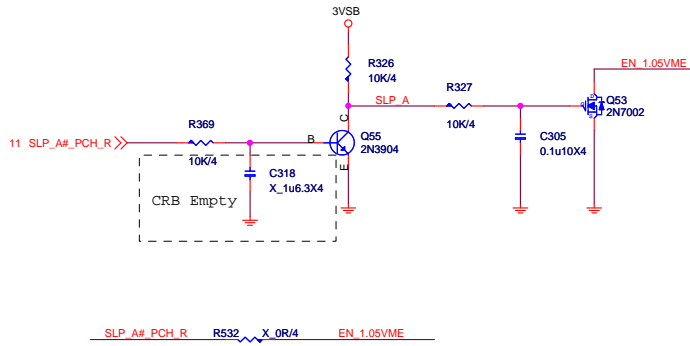
PCH Power:1.5V



VCC1\_5\_CTRL\_INPUT:  
0:1P05V low or S3 low  
1:1P05V HIGH and S3 HIGH

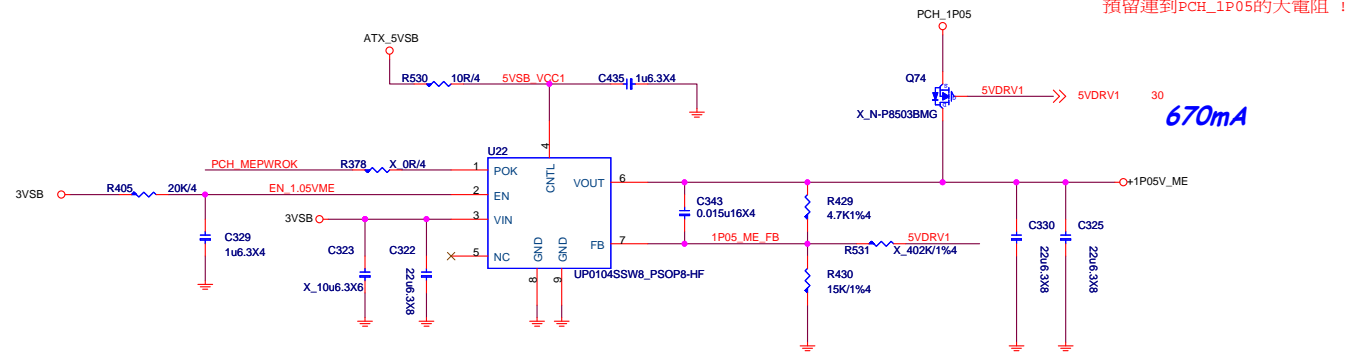


## SLP\_A

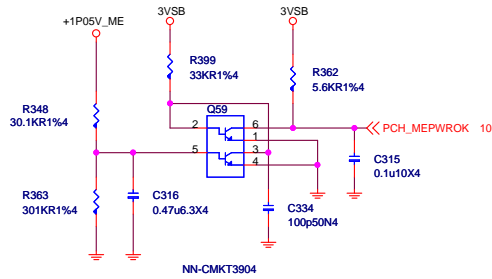


## ME Power Control

## +1.05V\_ME(VCCIO\_ME)

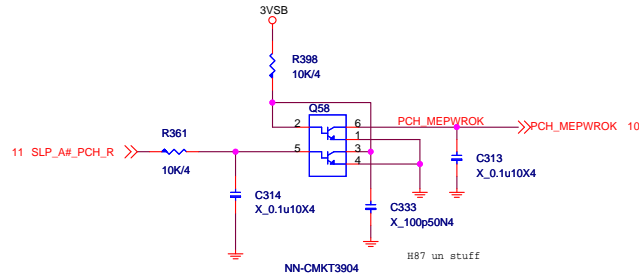
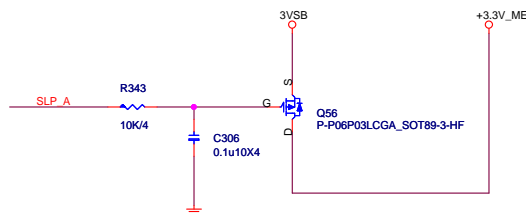


## PCH\_MEPWROK



VccASW active to APWROK high 1ms

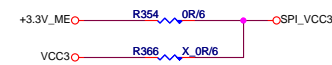
## +3.3V\_ME



APWROK falling to VccASW falling 40ns

For INTEL ME BUG

Z87->Stuff R366  
H87->Stuff R354

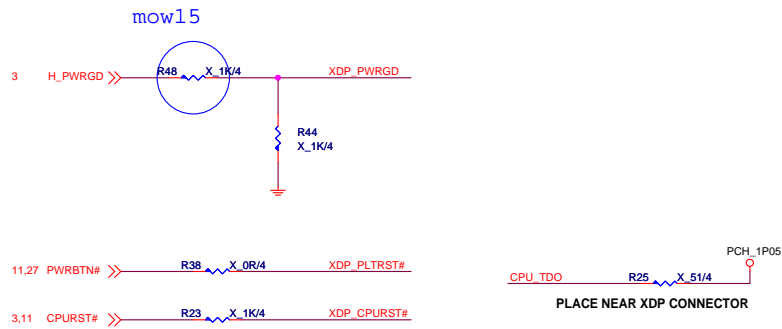
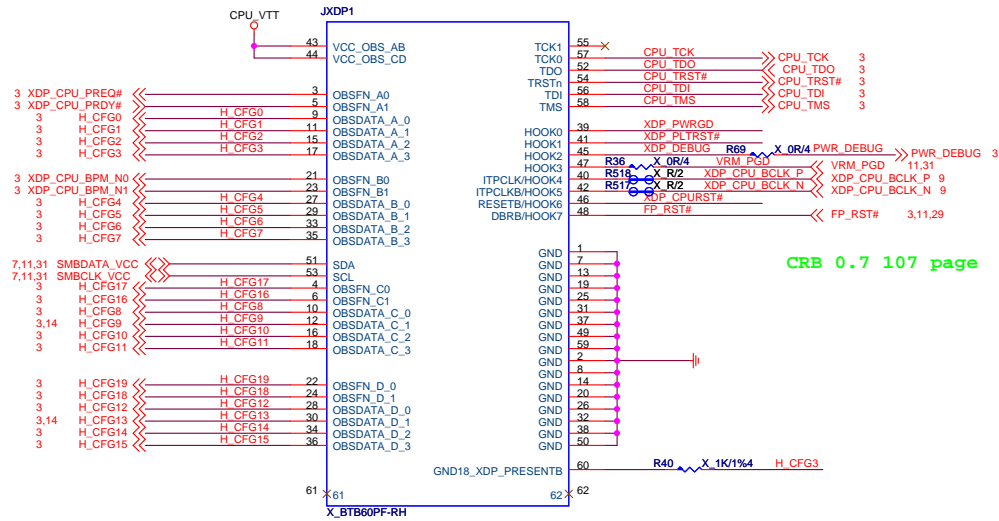


MICRO-STAR INT'L CO.,LTD

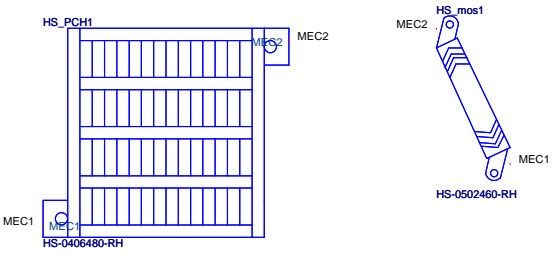
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## Reserve debug port 5020

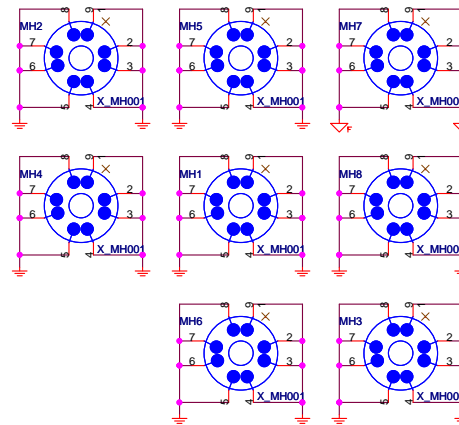


## HEATSINK



PK0-0782311-G37, 精成, 23, 寶安恩斯邁廠 (MSIS)  
PK0-0782311-G37, 精成, 77, 寶安恩斯邁廠 (MSIS)  
PK0-0782311-E48, 競華, 23, 寶安恩斯邁廠 (MSIS)  
PK0-0782311-E48, 競華, 77, 寶安恩斯邁廠 (MSIS)

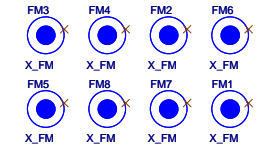
## Mounting Holes



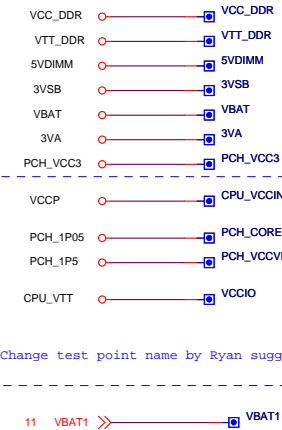
## Simulation



## Optical Fiducial Marks-120



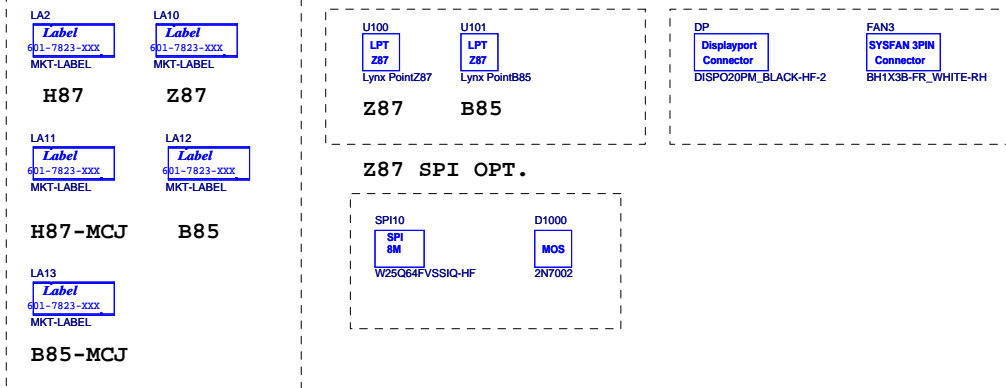
## Test point



## Label OPT.

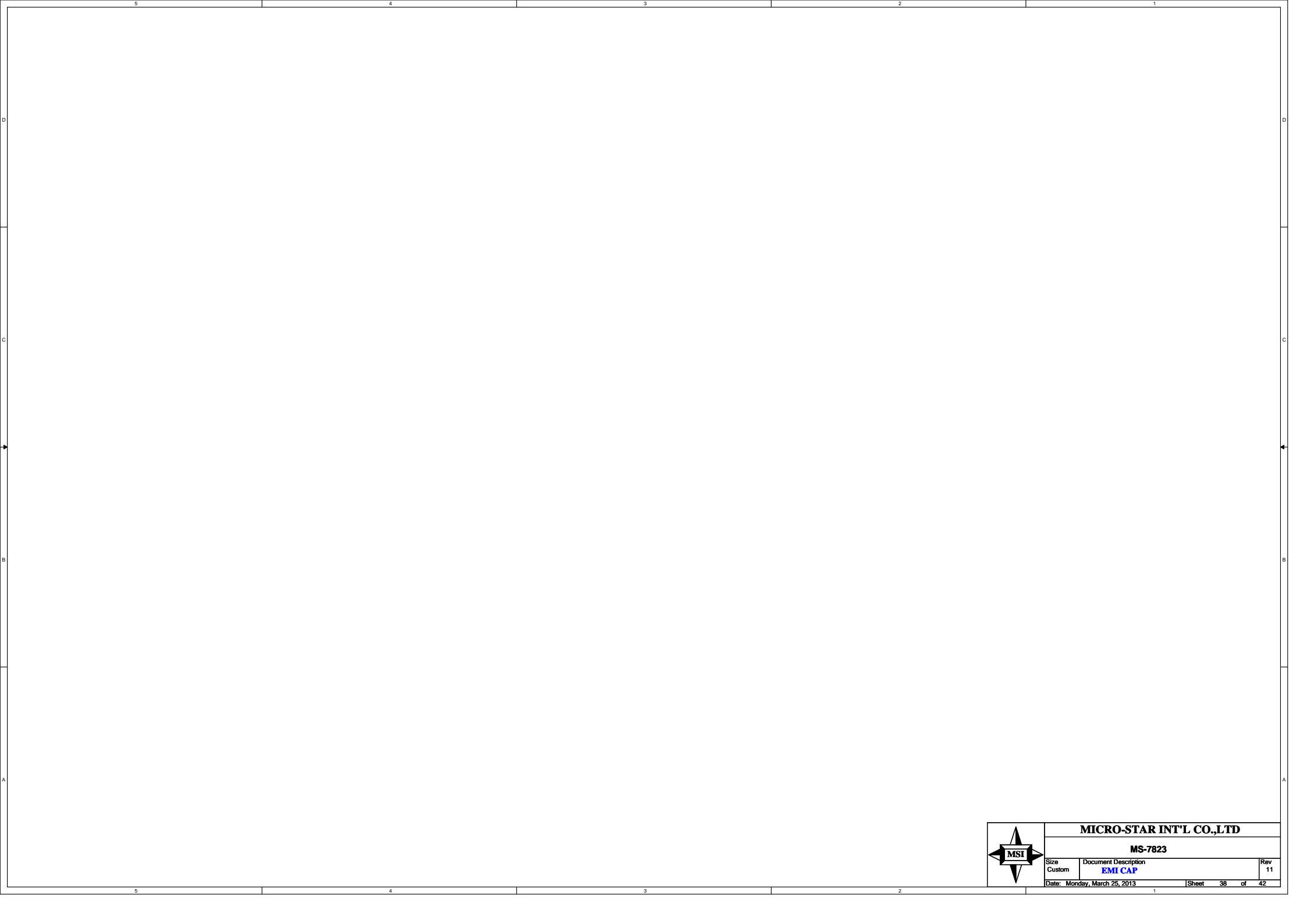
## Chip OPT.

## MCJ OPT.



## MS-7823-1.1 主BOM為H87

OPT	Configure	BOM	Function	GPIO Setting(GP10/GP11/GP12)
	H87M-G43	601-7823-04S	MS-7823 11 H87 H87M-G43, H87, LGA1150, 4DDR3, 2PCI-Ex16, 2PCI-Ex1 6SATA3, 4USB3, HD Audio, Gb LAN, HDMI, DP, DVI, D-Sub	0, 0, 0
A	Z87M-G43	601-7823-05S	MS-7823 11 OPT:A Z87 Z87M-G43, Z87, LGA1150, 4DDR3, 2PCI-Ex16, 2PCI-Ex1 6SATA3, 4USB3, HD Audio, Gb LAN, HDMI, DP, DVI, D-Sub	0, 0, 0
B	H87M-S01 (MCJ)	601-7823-06S	MS-7823 11 OPT:B H87 H87M-S01, H87, LGA1150, 4DDR3, 2PCI-Ex16, 2PCI-Ex1 6SATA3, 4USB3, HD Audio, Gb LAN, DP, DVI, D-Sub	1, 0, 0
C	B85M-G43	601-7823-07S	MS-7823 11 OPT:C B85 B85M-G43, B85, LGA1150, 4DDR3, 2PCI-Ex16, 2PCI-Ex1 4SATA3, 4USB3, HD Audio, Gb LAN, HDMI, DP, DVI, D-Sub	0, 0, 0
D	B85M-S01 (MCJ)	601-7823-08S	MS-7823 11 OPT:D B85 B85M-S01, B85, LGA1150, 4DDR3, 2PCI-Ex16, 2PCI-Ex1 4SATA3, 4USB3, HD Audio, Gb LAN, DP, DVI, D-Sub	1, 0, 0



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